

KL3A Intel Calpella Platform with Discrete GFX(4 core)

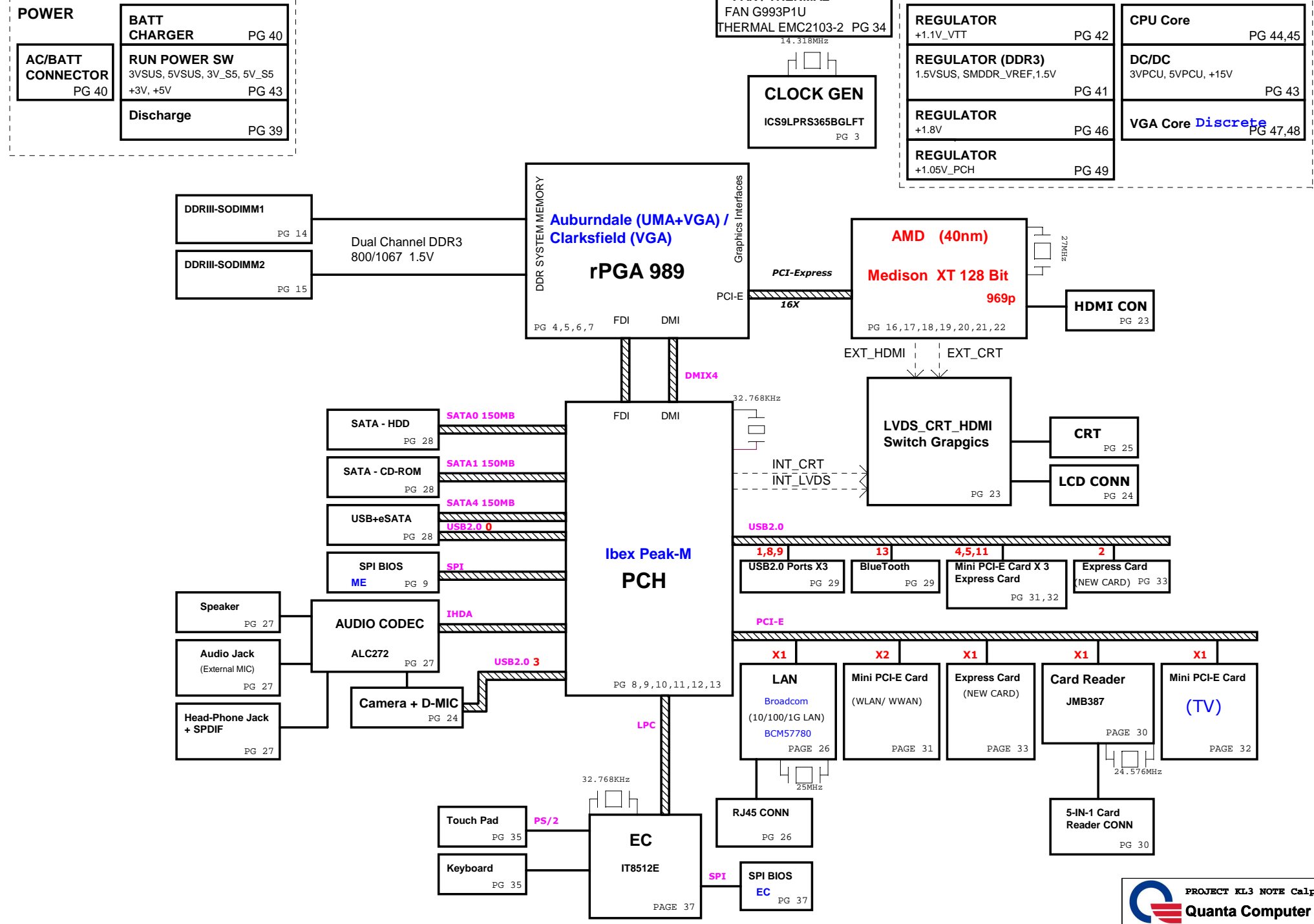
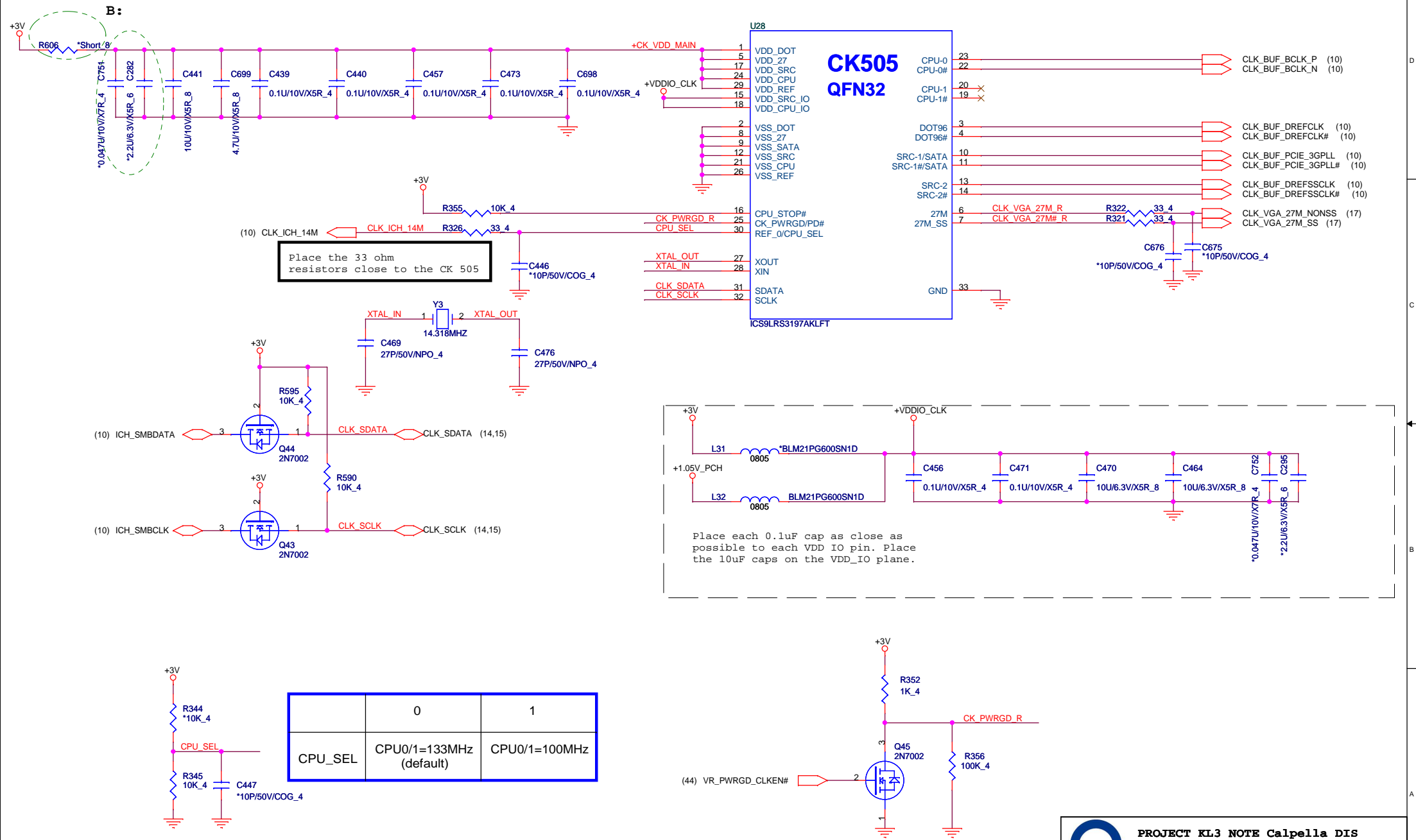


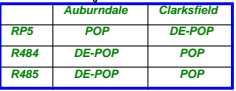
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Power States

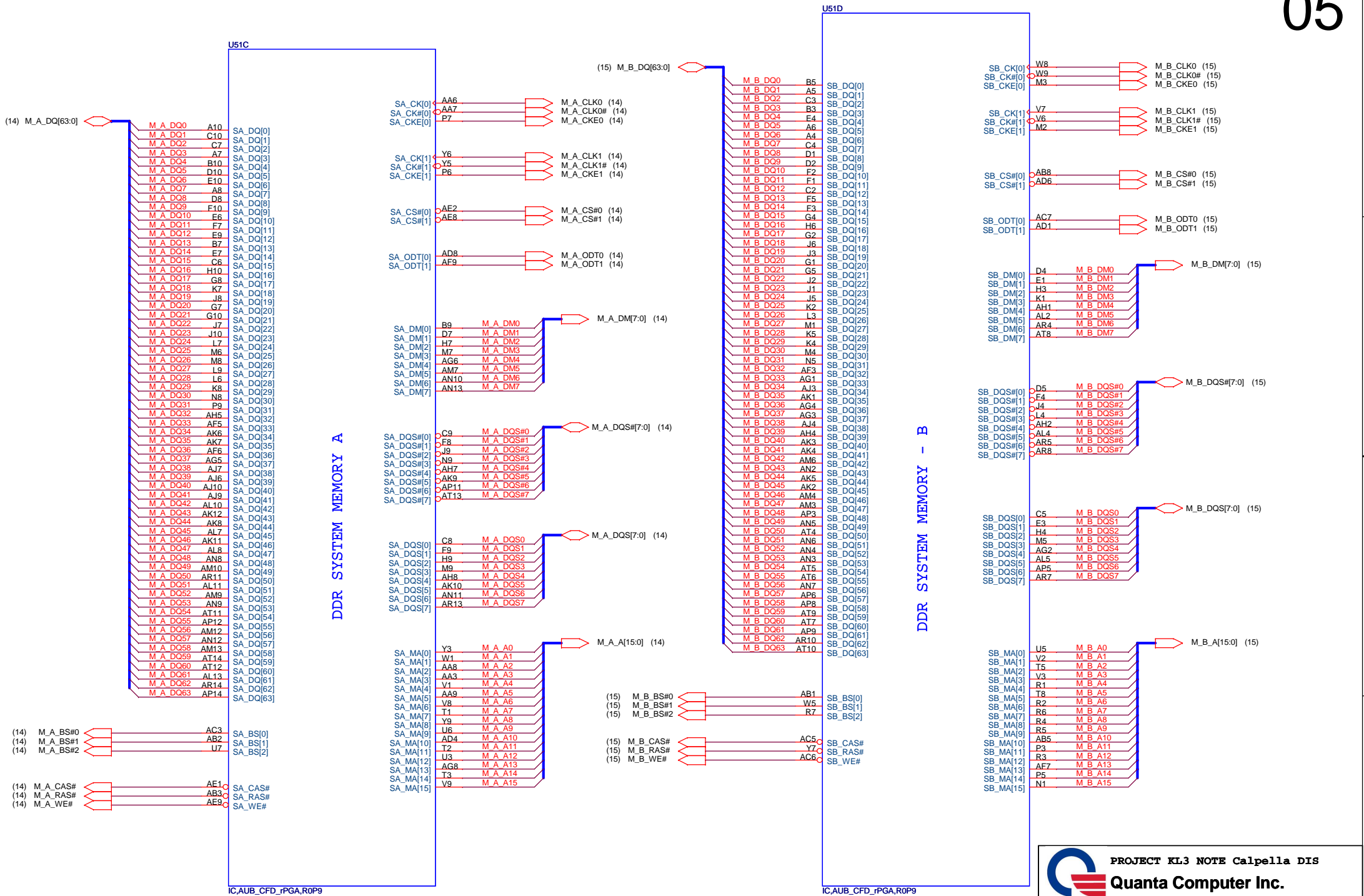
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0~S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well, Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0~S5

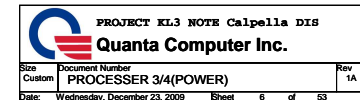


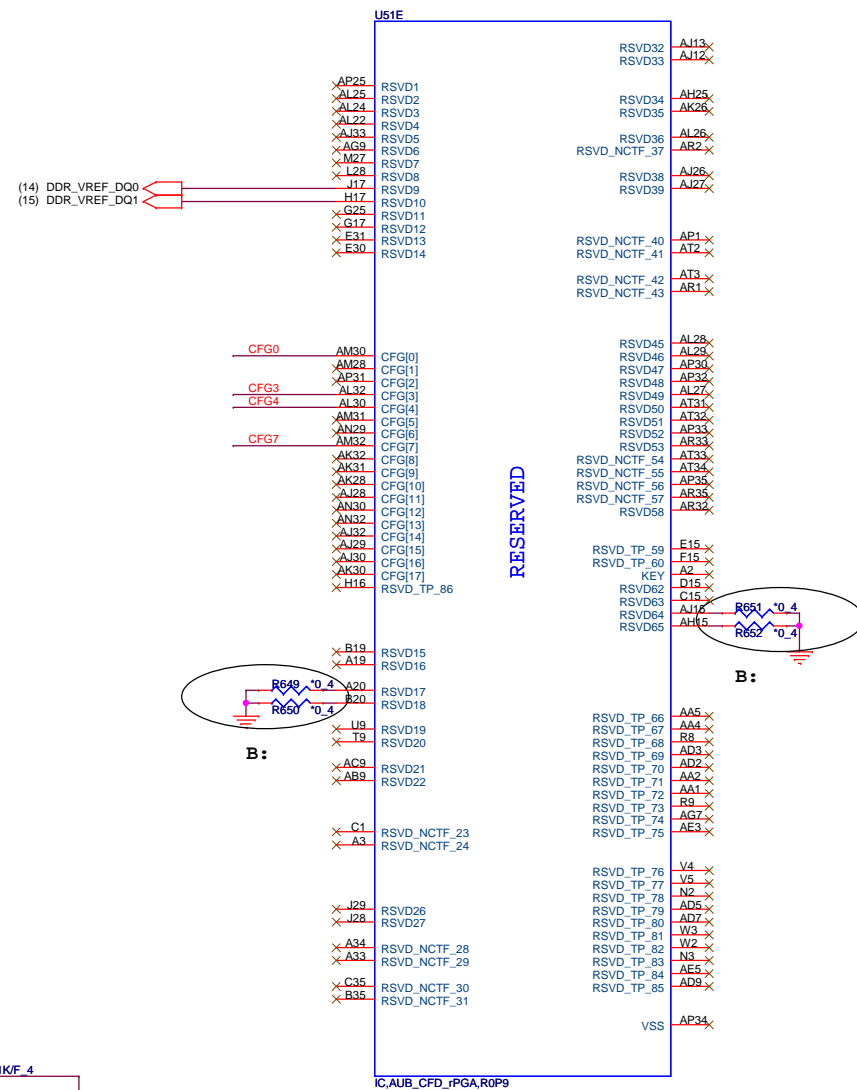


AUBURNDALE PROCESSOR (DDR3)

05






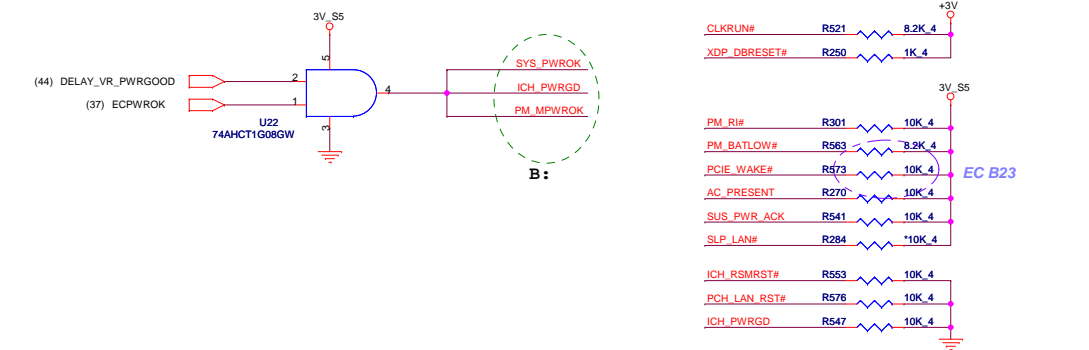
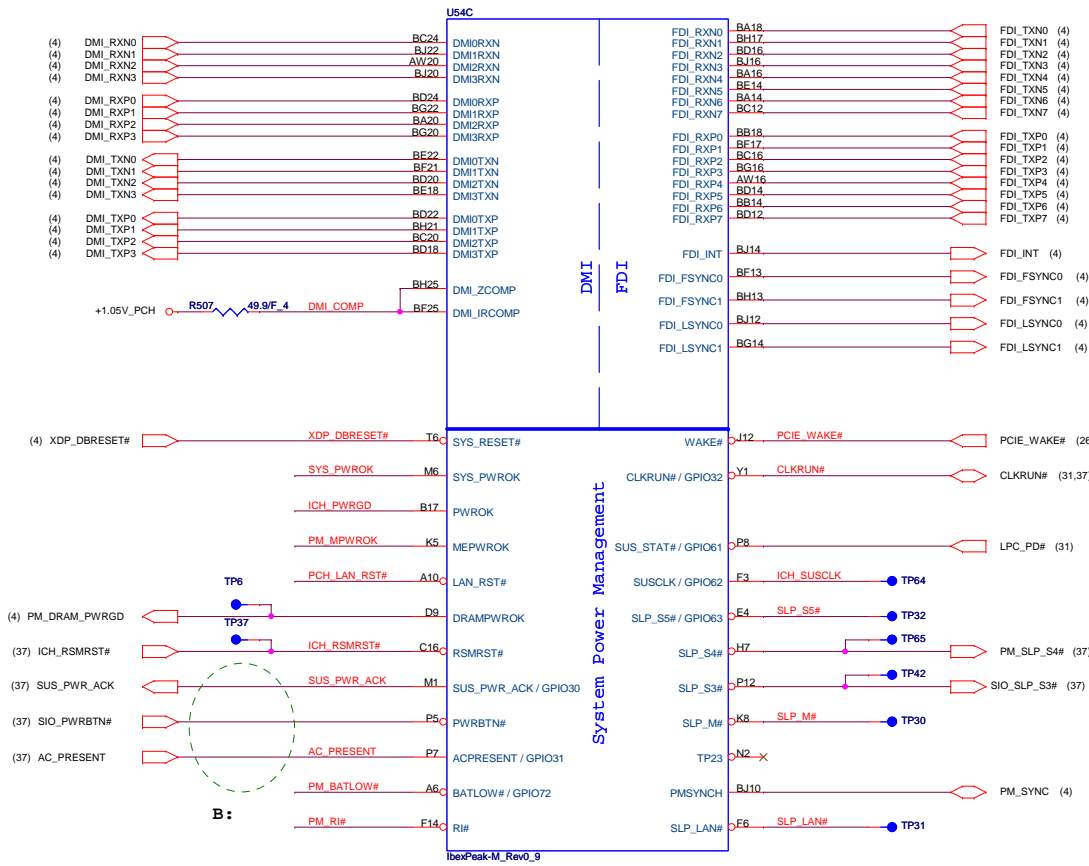


CFG4 R201 ~*3.01K/F 4
 CFG0 R202 ~*3.01K/F 4
 CFG3 R200 ~*3.01K/F 4
 CFG7 R133 ~*3.01K/F 4

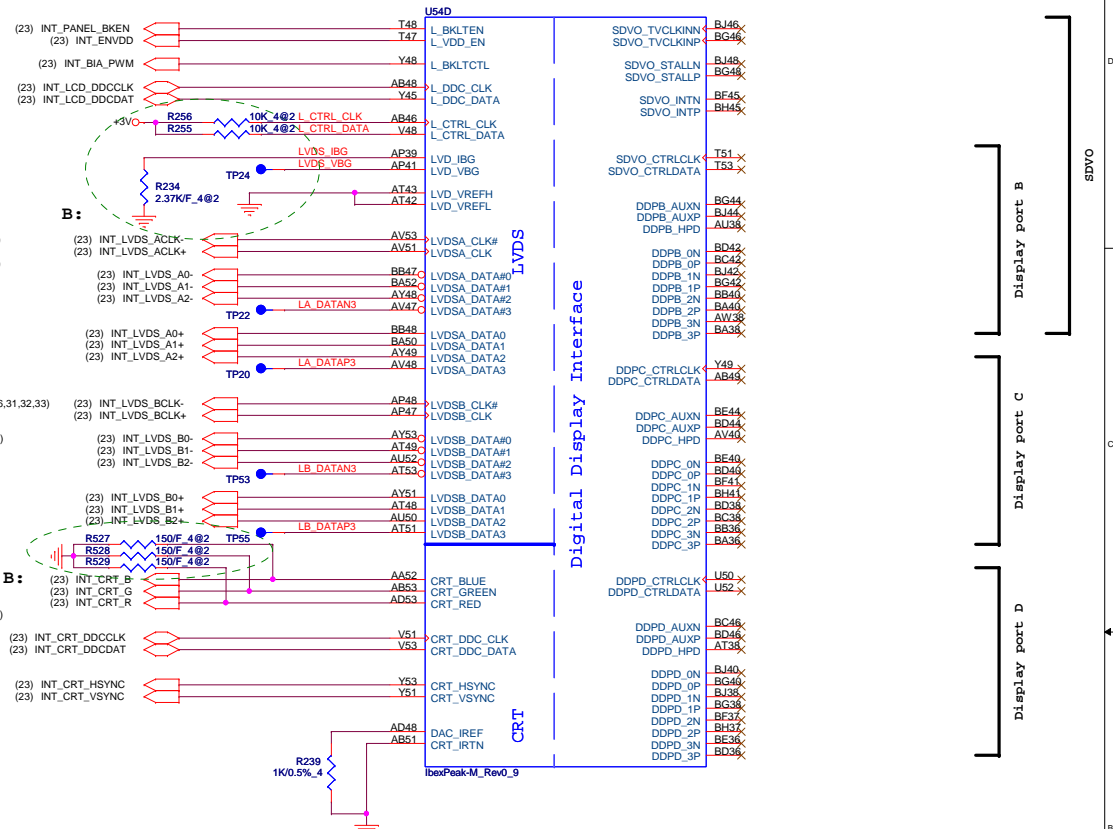
IC_AUB_CFG_rPGA,R0P9
 CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

	PROJECT KL3 NOTE Calpella DIS		
	Quanta Computer Inc.		
Size Custom	Document Number PROCESSOR 4/4(GND)		Rev 1A
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IBEX PEAK-M (DMI, FDI, GPIO)



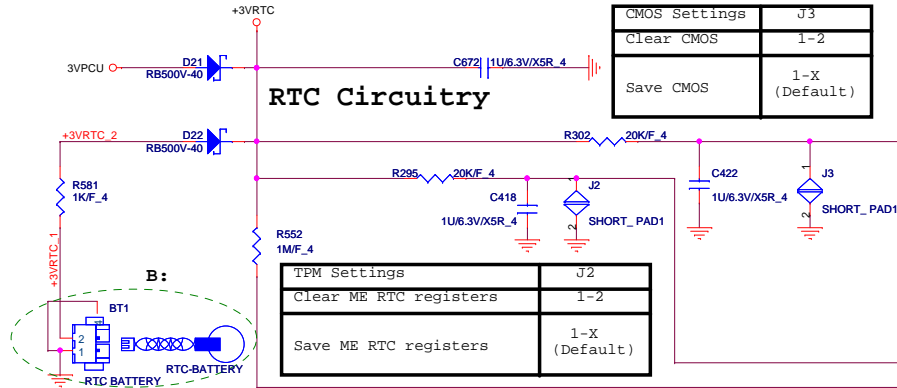
IBEX PEAK-M (LVDS, DDI)



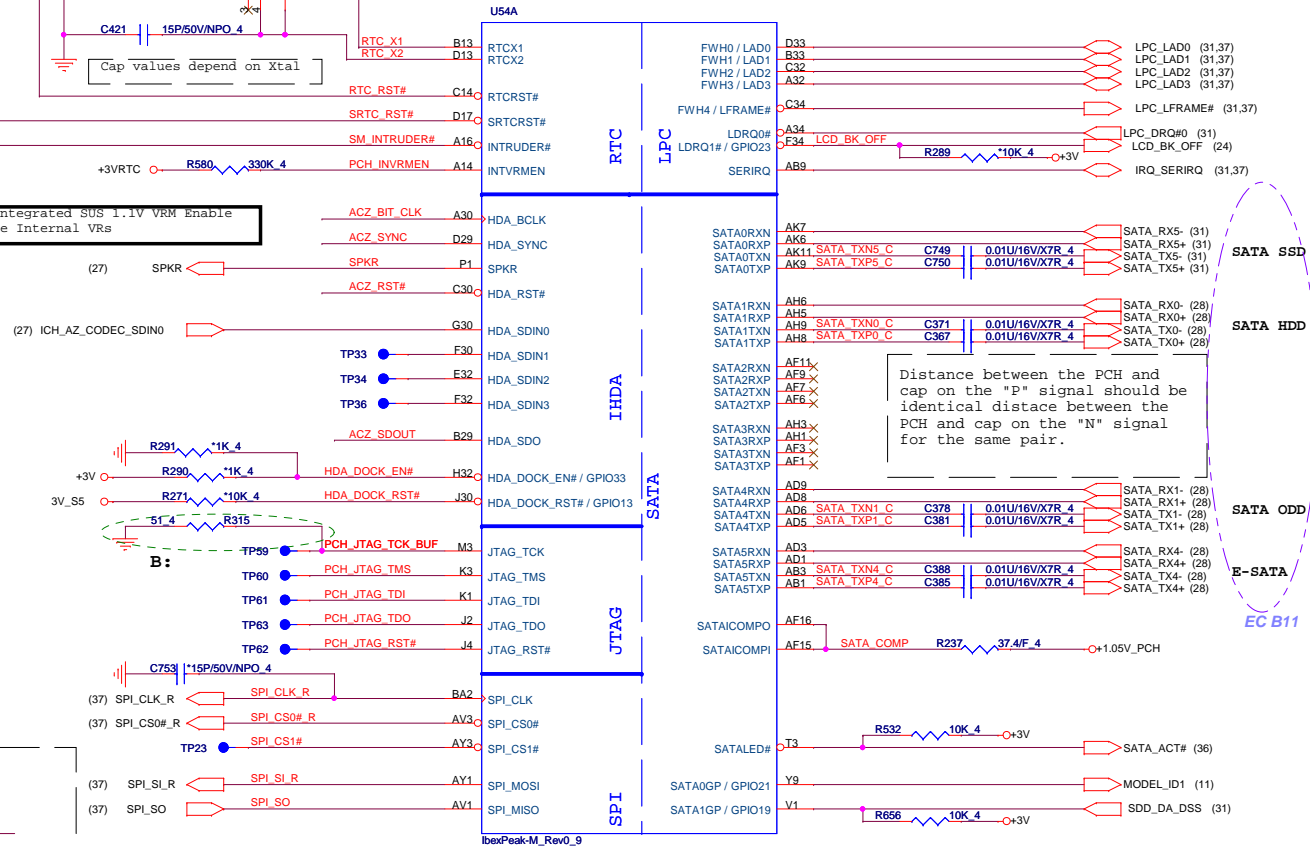
	Auburndale	Clarksfield
R256	POP	DE-POP
R255	POP	DE-POP
R234	POP	DE-POP
R527	POP	DE-POP
R528	POP	DE-POP
R529	POP	DE-POP

RTC Circuitry

CMOS Settings	J3
Clear CMOS	1-2
Save CMOS	1-X (Default)

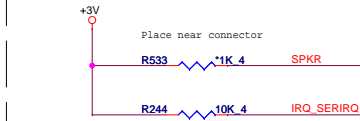


IBEX PEAK-M (HDA,JTAG,SATA)



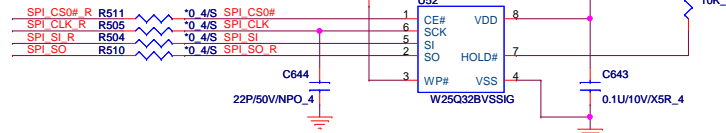
Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot Strap



For PCH

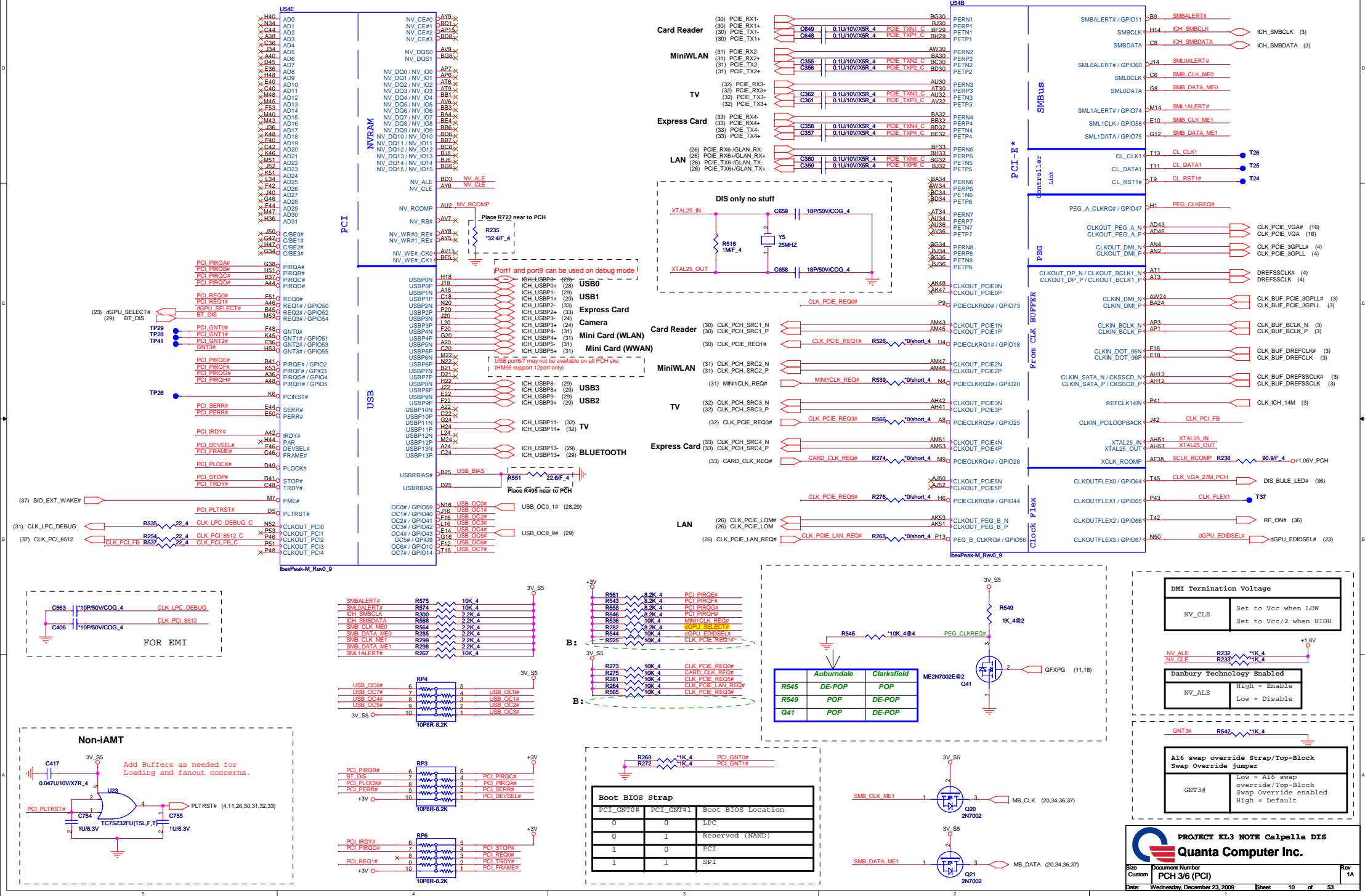
16Mbit (2M Byte), SPI



iTPM ENABLE/DISABLE



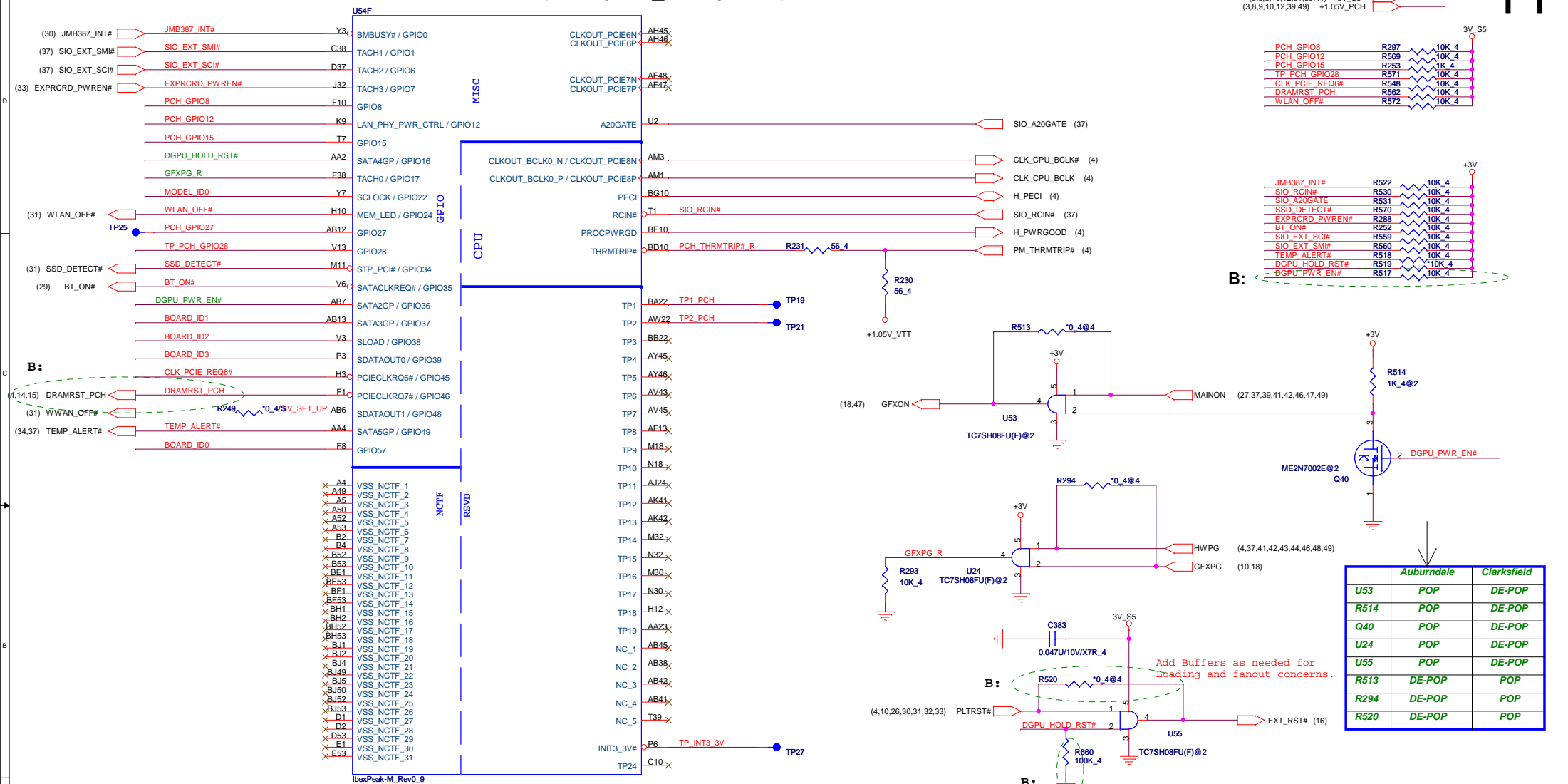
TPM Function	R9386
Enable	Stuff
Disable	NC (Default)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

(3,4,8,9,10,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,44,47) +3V
(6,8,9,10,12,31,39,41) 3V_S5
(3,8,9,10,12,38,49) +1.05V_PCH

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B:

	Auburndale	Clarksfield
U53	POP	DE-POP
R514	POP	DE-POP
Q40	POP	DE-POP
U24	POP	DE-POP
U55	POP	DE-POP
R513	DE-POP	POP
R294	DE-POP	POP
R520	DE-POP	POP

Board ID

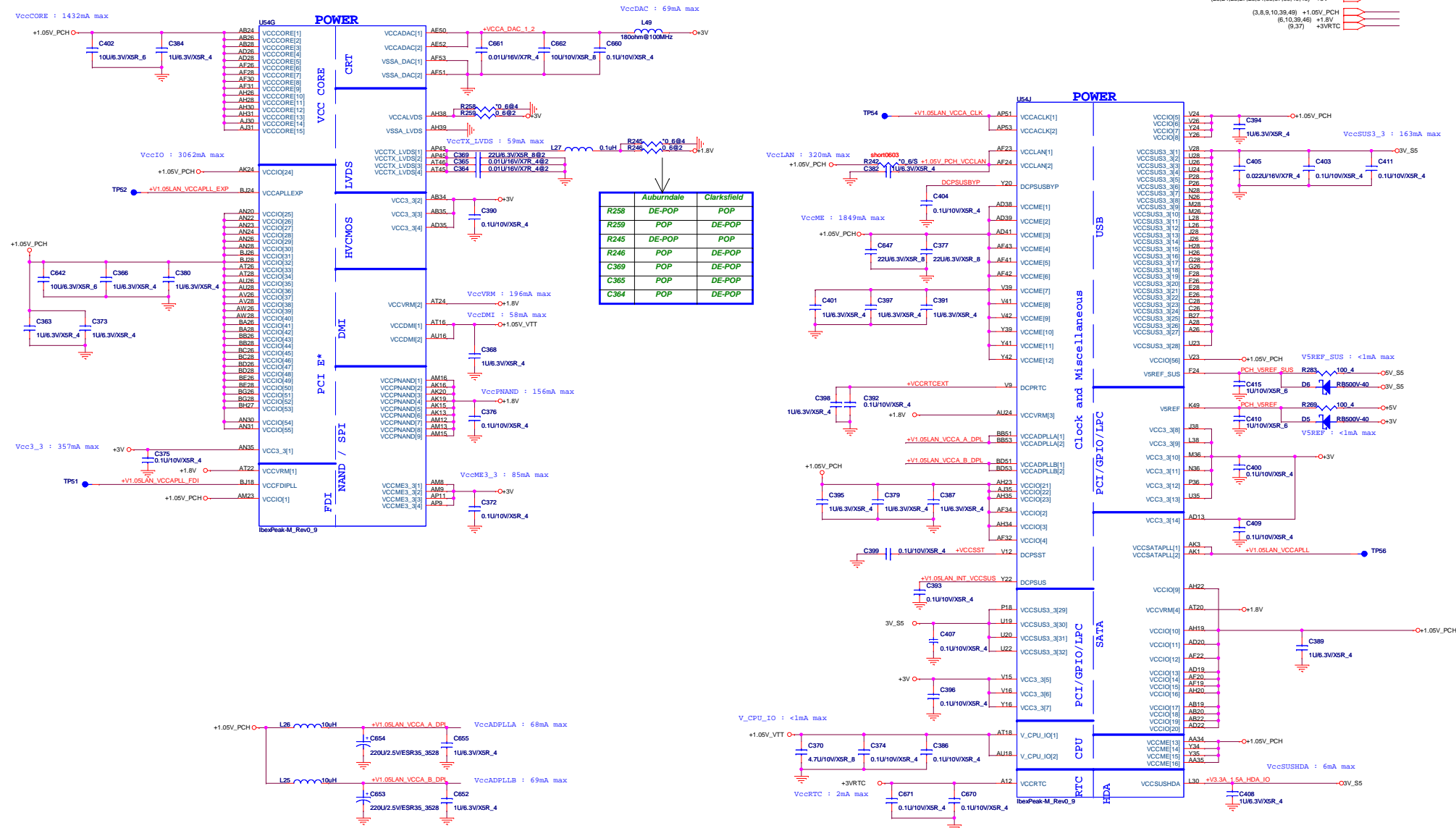
Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO35
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	1	0	0
SOVP	1	0	0	0

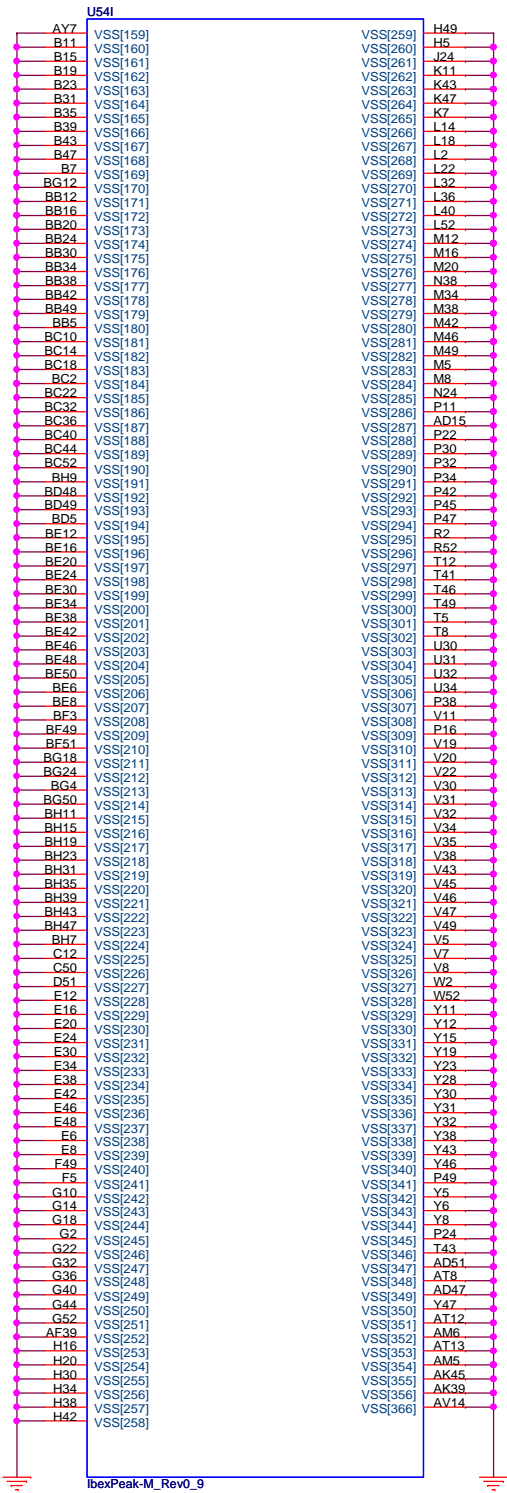
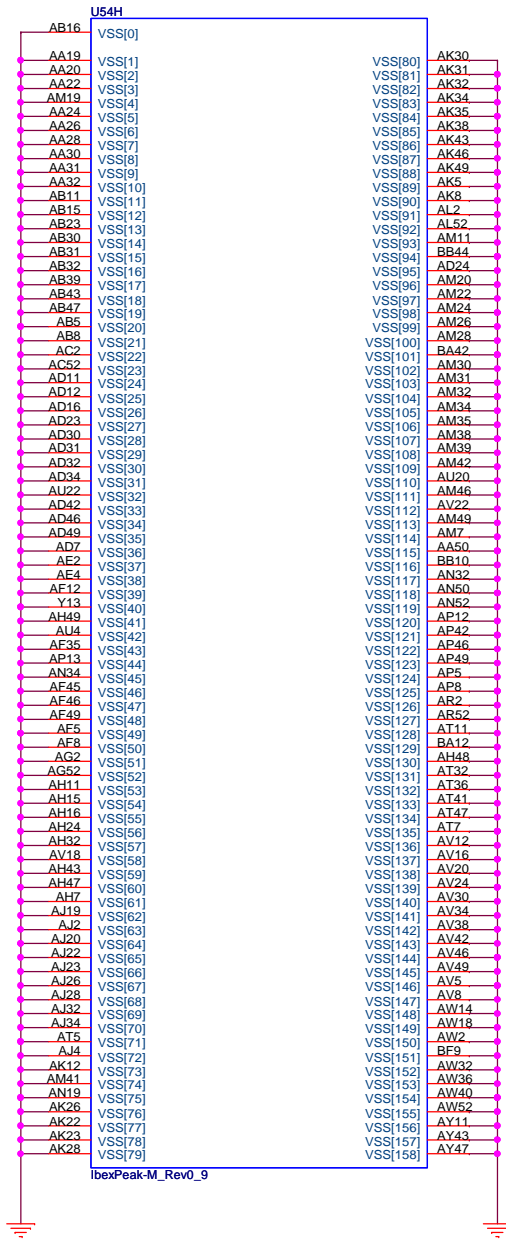
Model ID

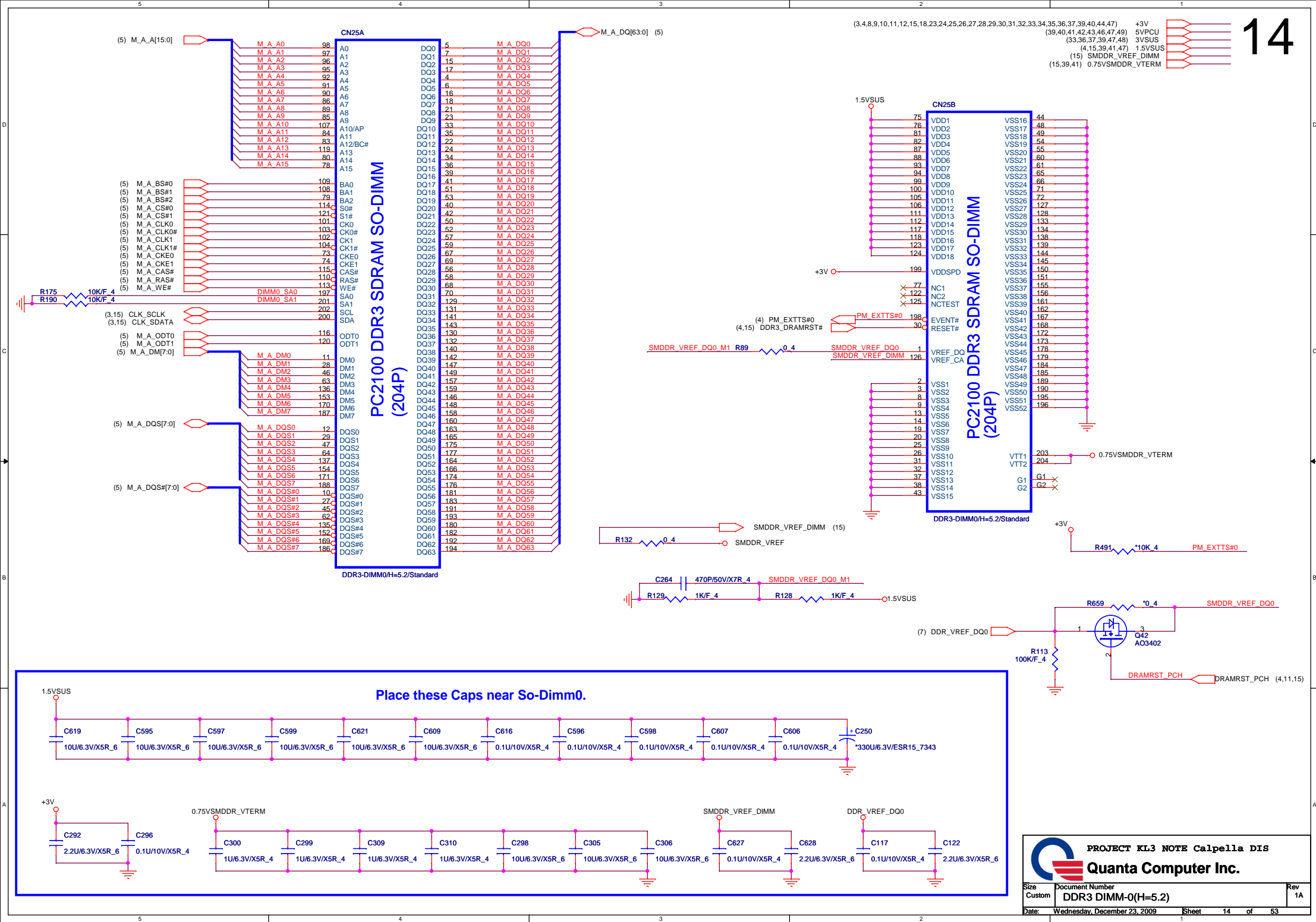
Model ID	MODEL_ID0	MODEL_ID1
14"	0	1
15"	1	0
Default	1	1

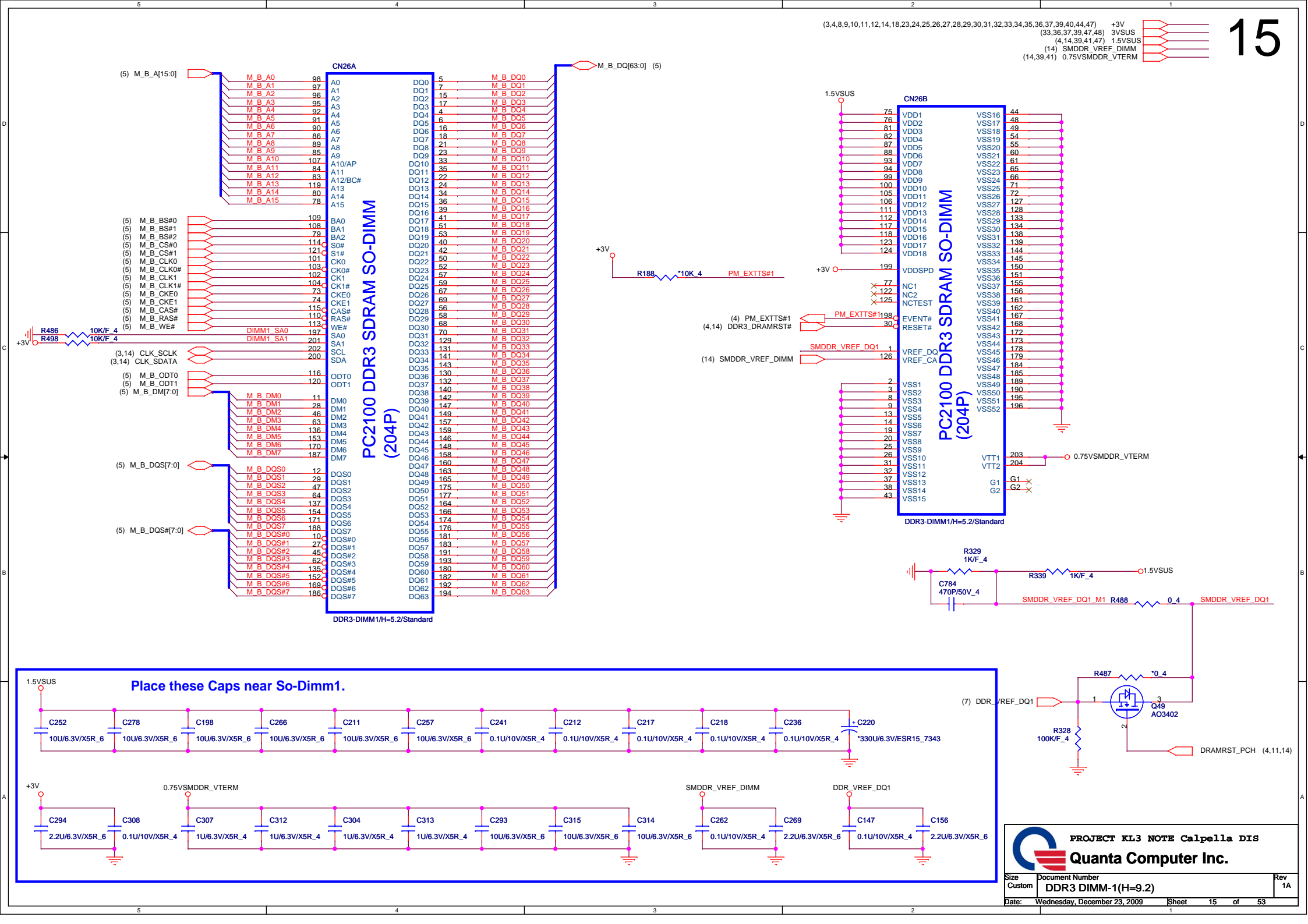
PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

Size Custom Document Number PCH 4/6 (GPIO)
 Date: Wednesday, December 23, 2009 Sheet 11 of 53

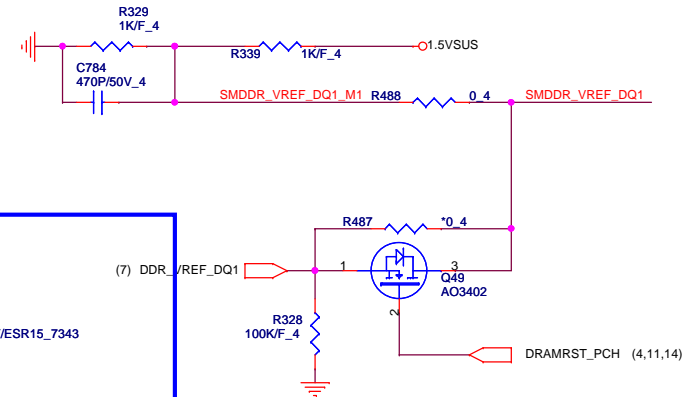
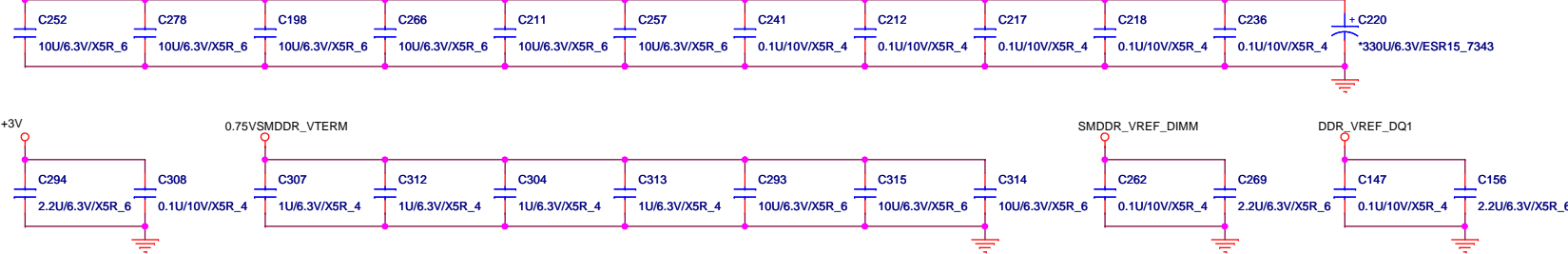


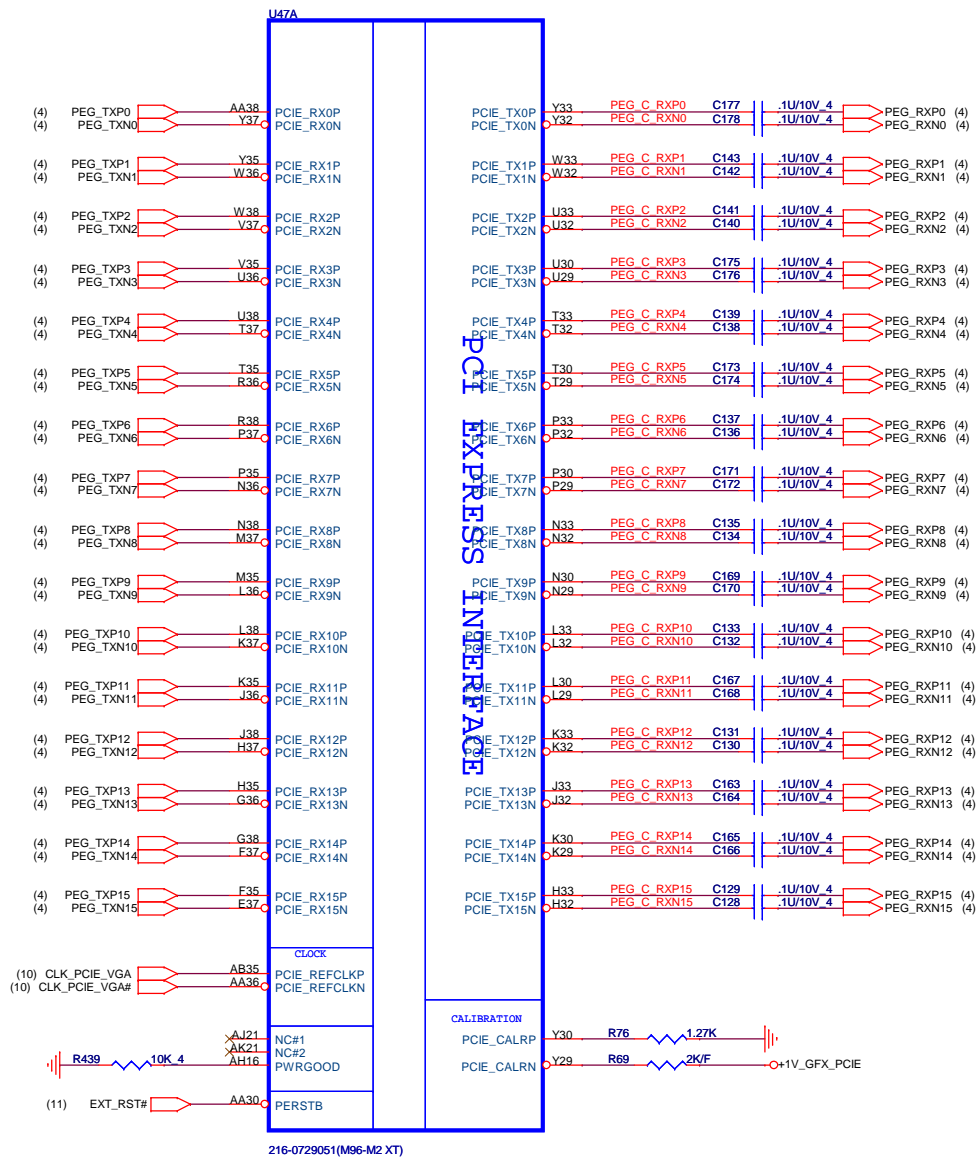






Place these Caps near So-Dimm1.





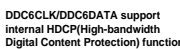
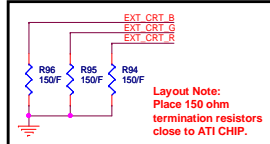
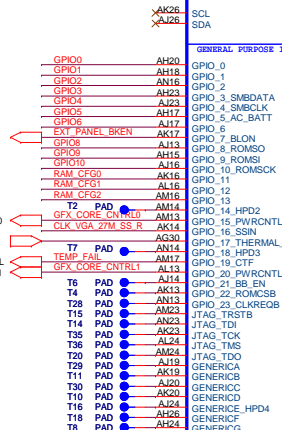
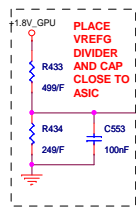
Note : Required Frequency = 800 MHz



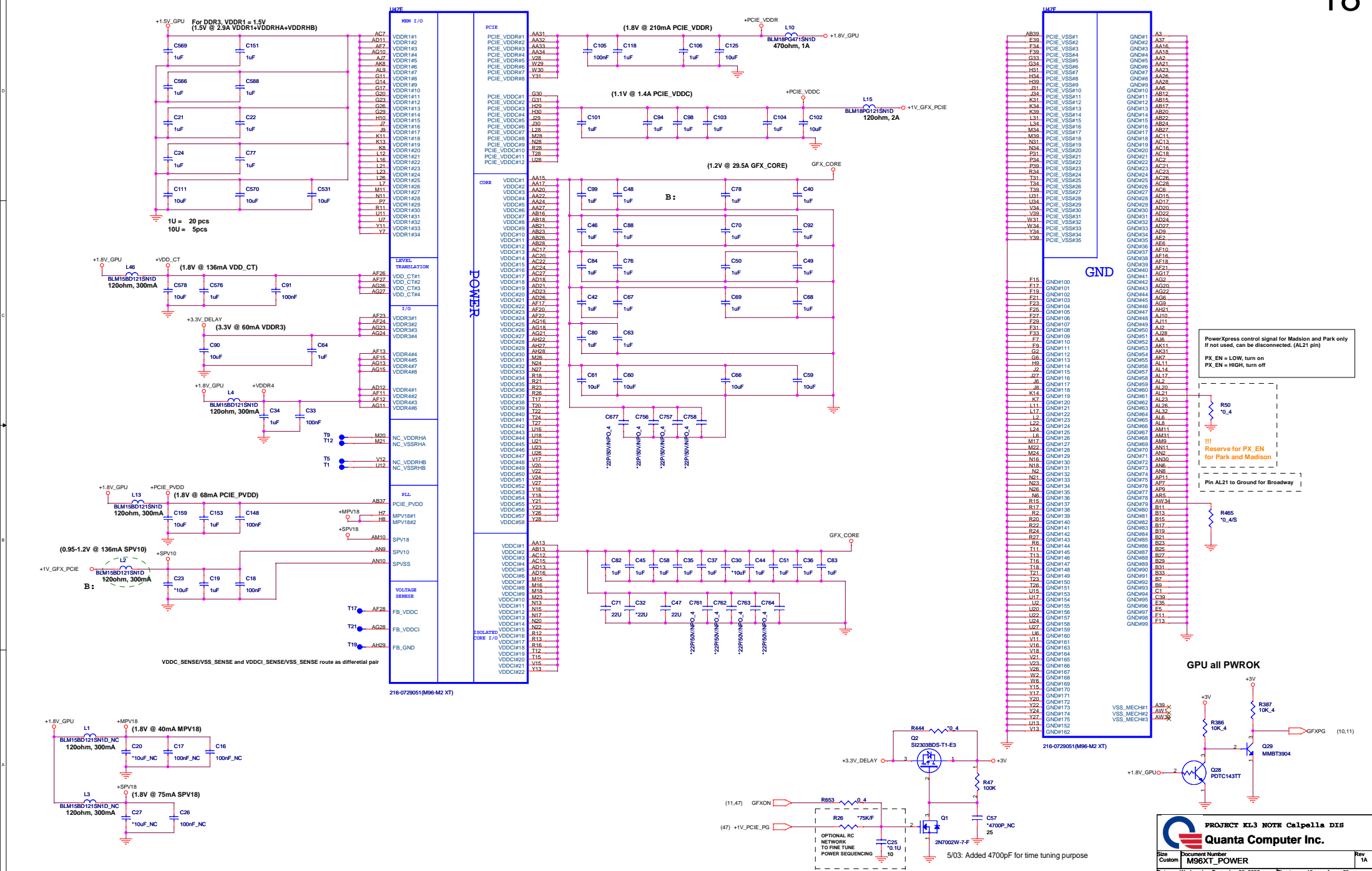
Pin	Signal	Function
R435	*10K 4	GFX CORE CNTRL0
R298	*10K 4	GFX CORE CNTRL1
R48	10K 4	GPIO0
R41	10K 4	GPIO1
R35	*10K 4	GPIO2
R60	*10K 4	GPIO3
R55	*10K 4	GPIO4
R37	*10K 4	GPIO5
R45	*10K 4	GPIO6
R28	*10K 4	GPIO8
R31	*10K 4	GPIO9
R34	*10K 4	GPIO10
R69	10K 4	EXT CRT HSYNC
R98	10K 4	EXT CRT VSYNC
R73	*10K 4	VGAHSYNC2
R32	*10K 4	EXT PANEL BKEN



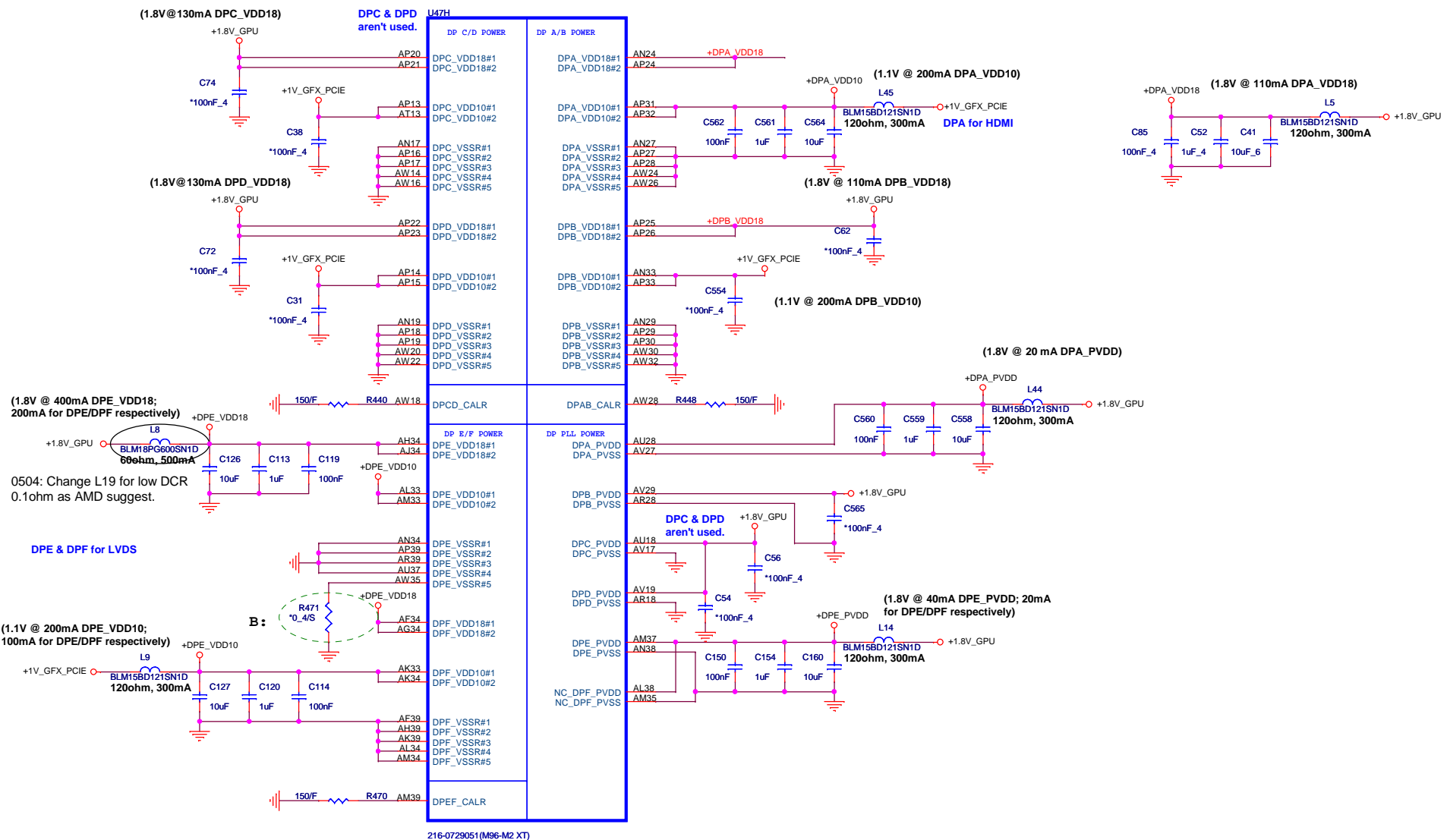
```
1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK
```



CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

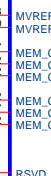


!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V



U47C

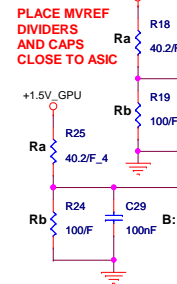
MEMORY INTERFACE A



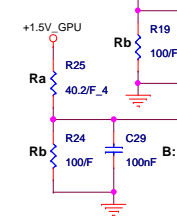
216-0729051(M96-M2 XT)

DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R



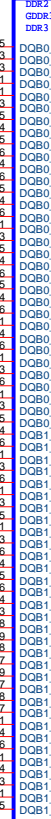
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



216-0729051(M96-M2 XT)

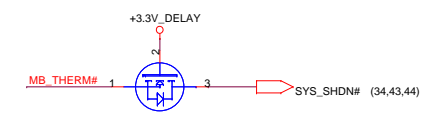
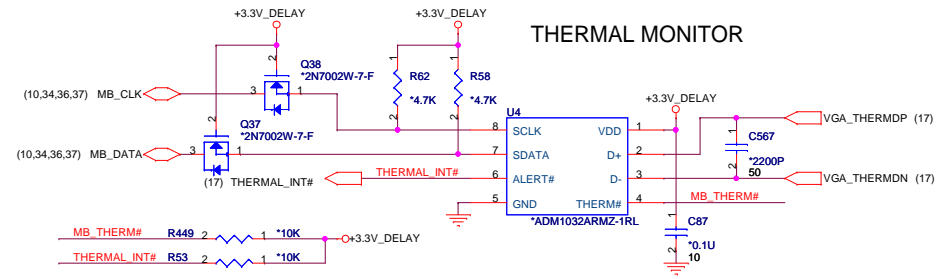
U47D

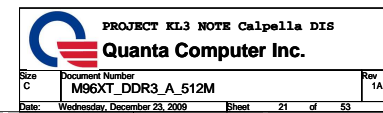
MEMORY INTERFACE B

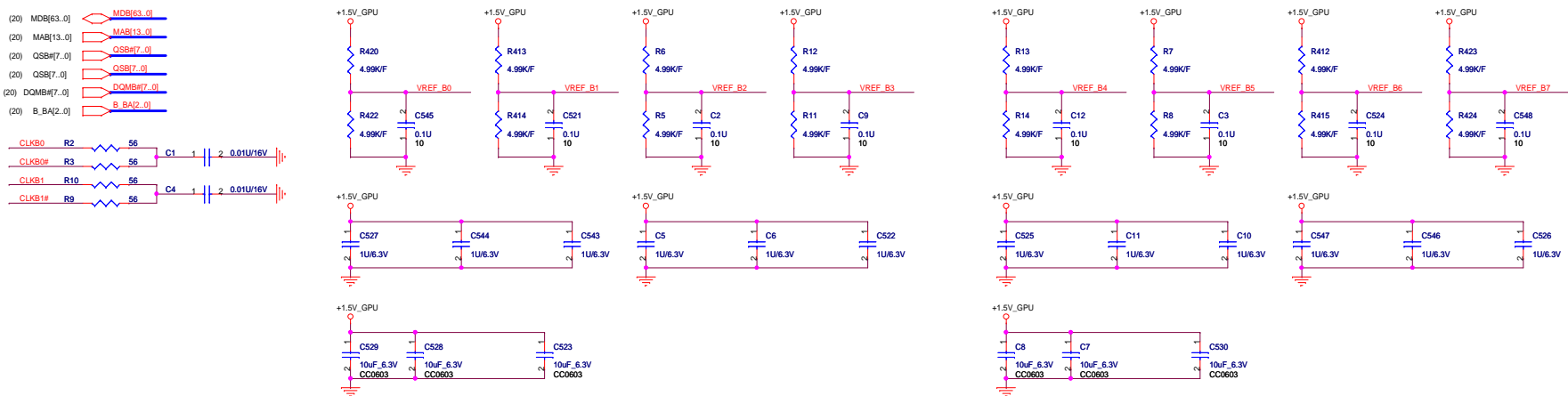


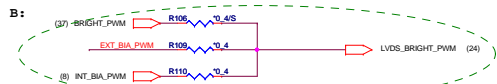
216-0729051(M96-M2 XT)

THERMAL MONITOR

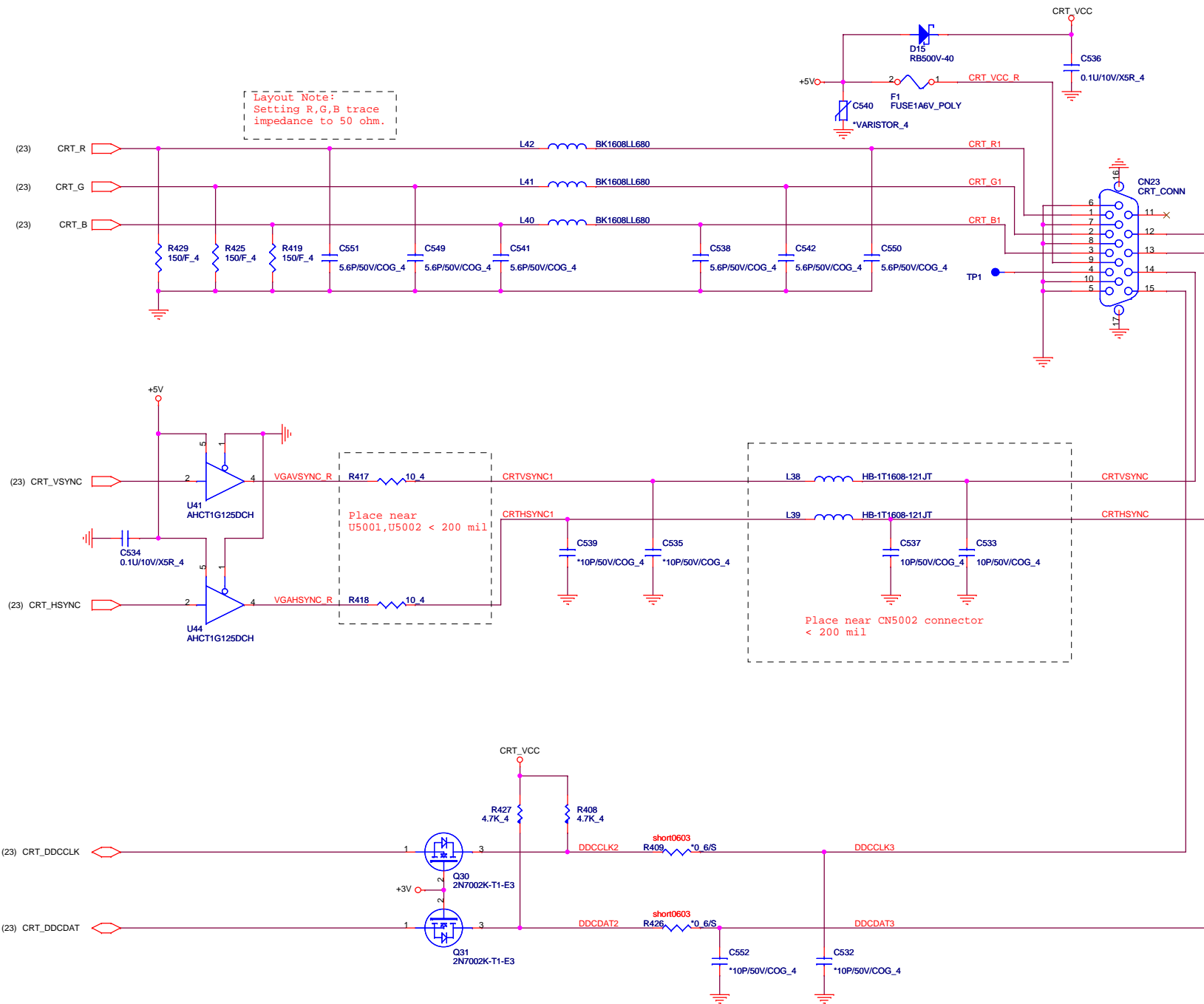


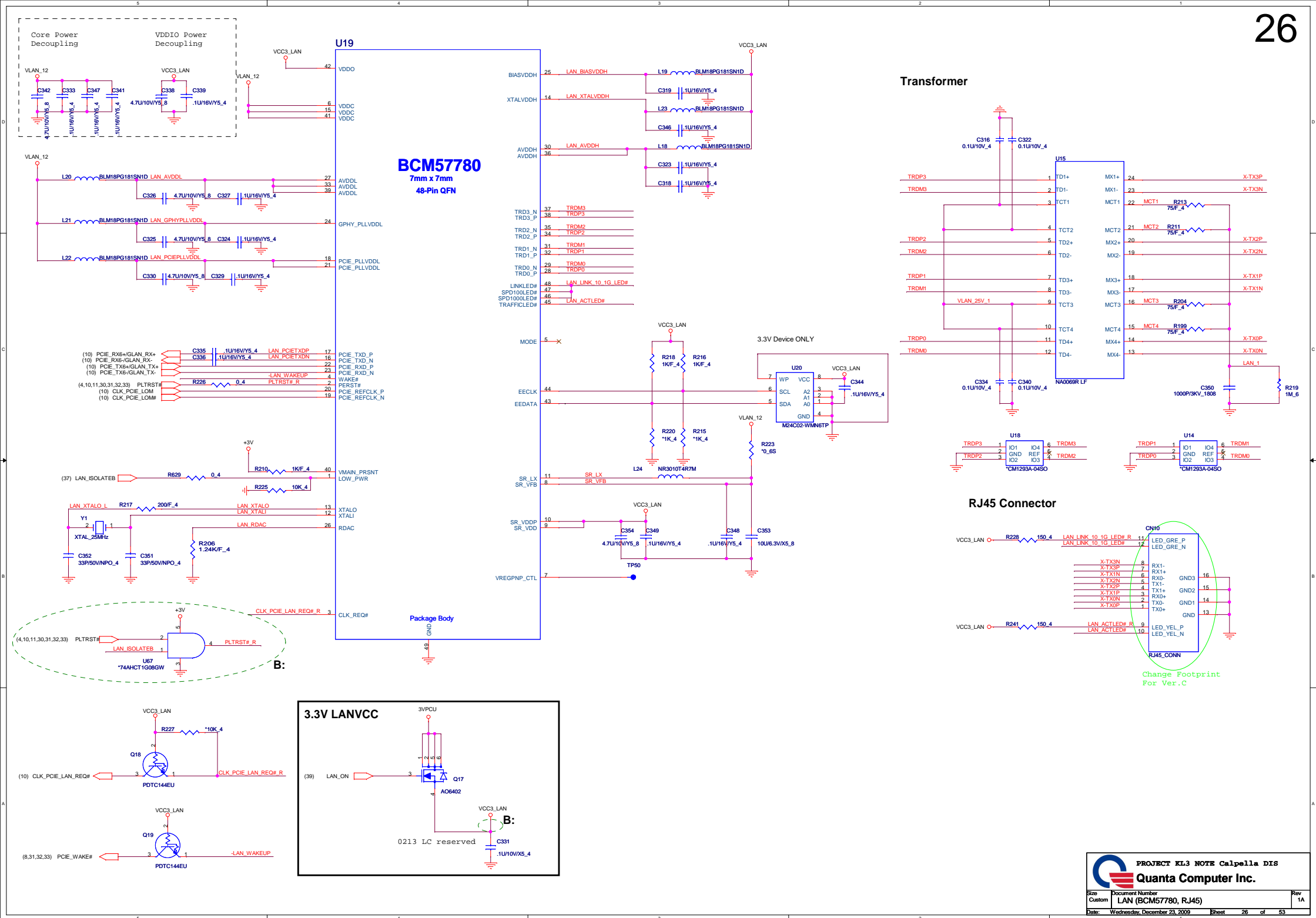




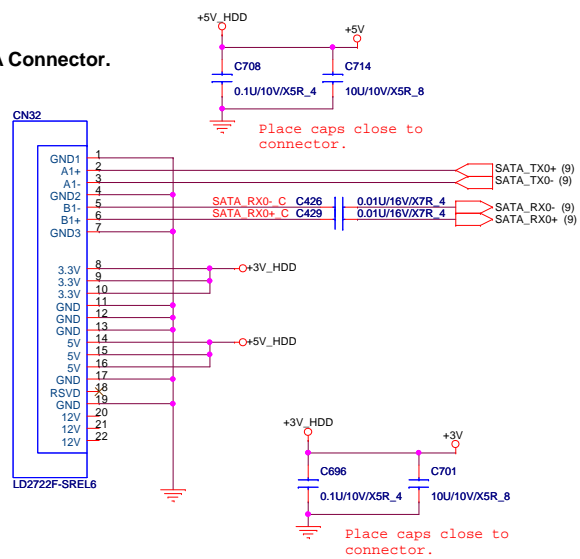




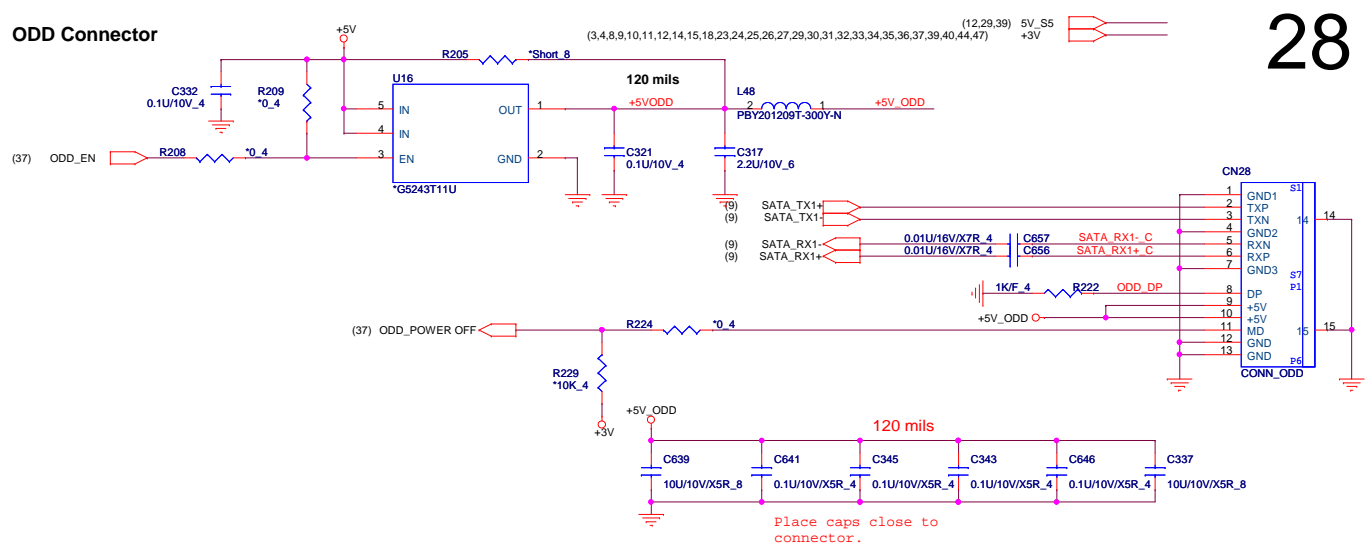




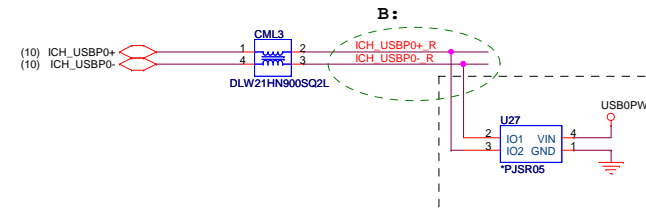
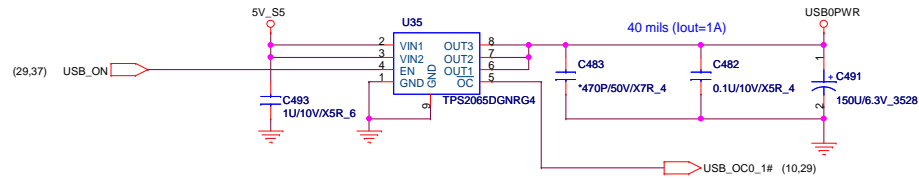
SATA Connector.



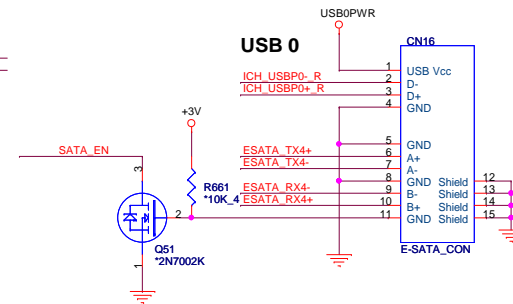
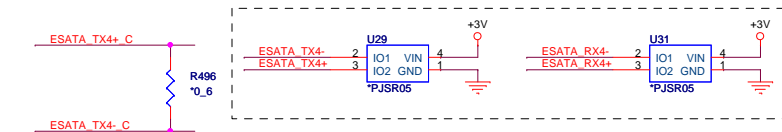
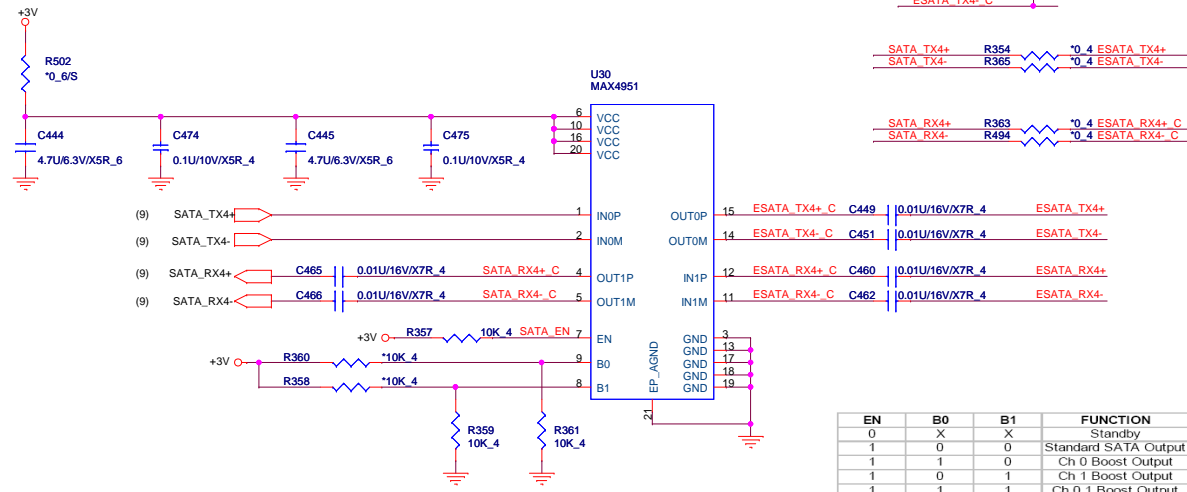
ODD Connector



USB + E-SATA

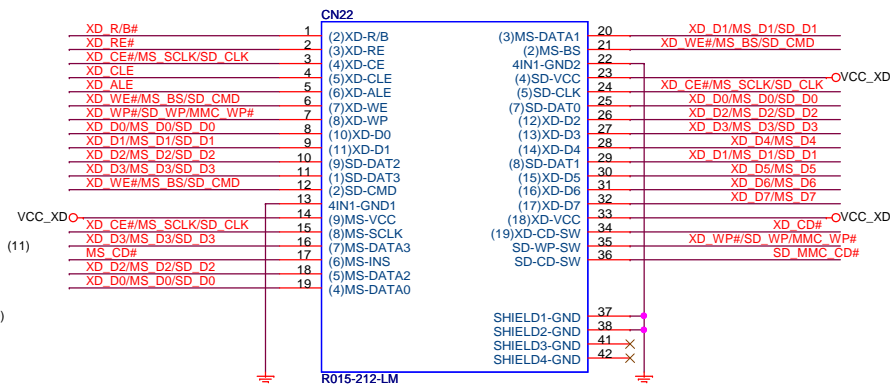
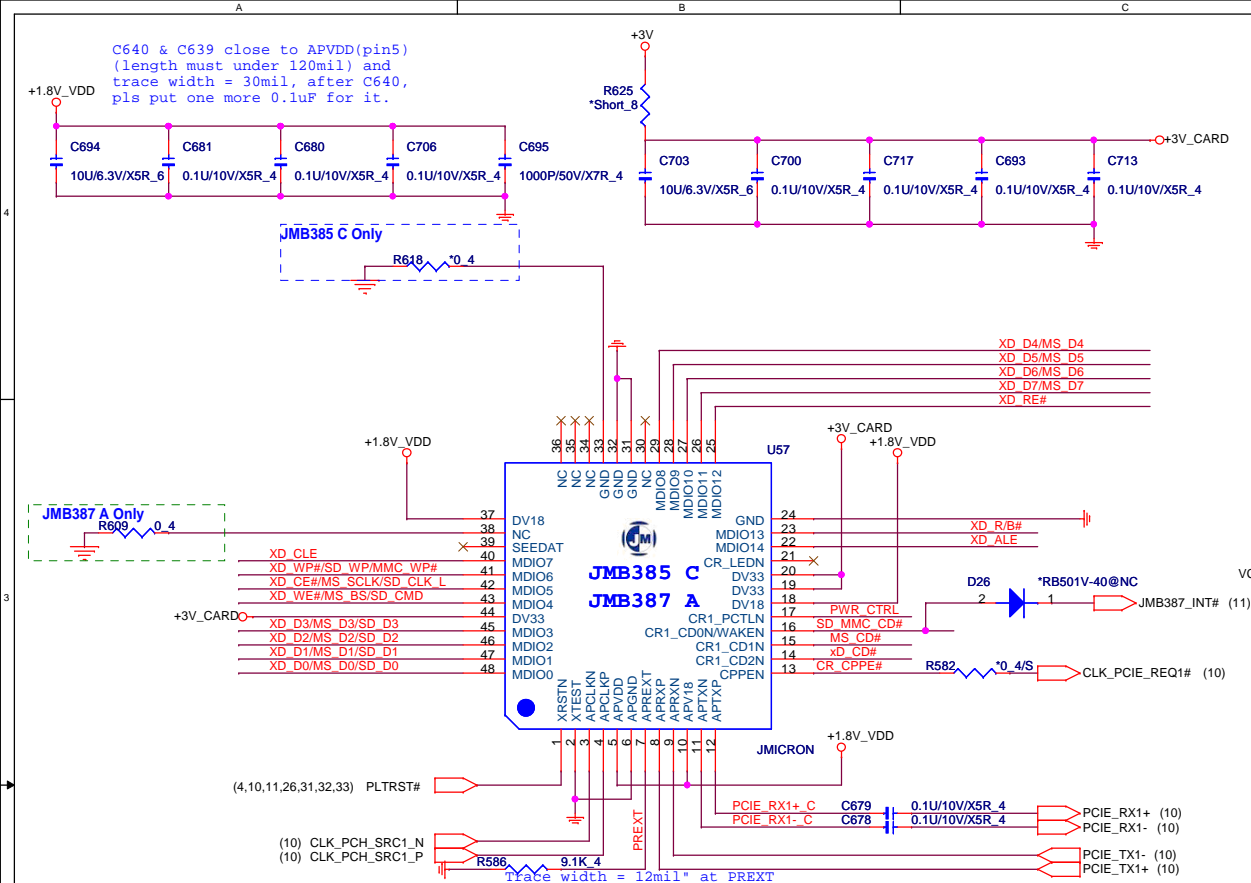


E-SATA RE-DRIVER

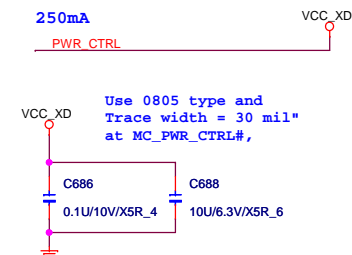
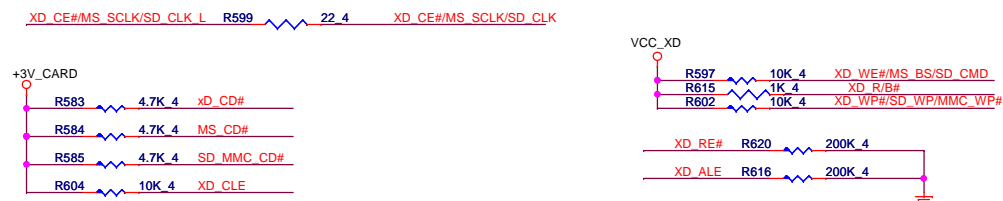


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

5 IN 1 CARD READER



Memory Card Power Supply

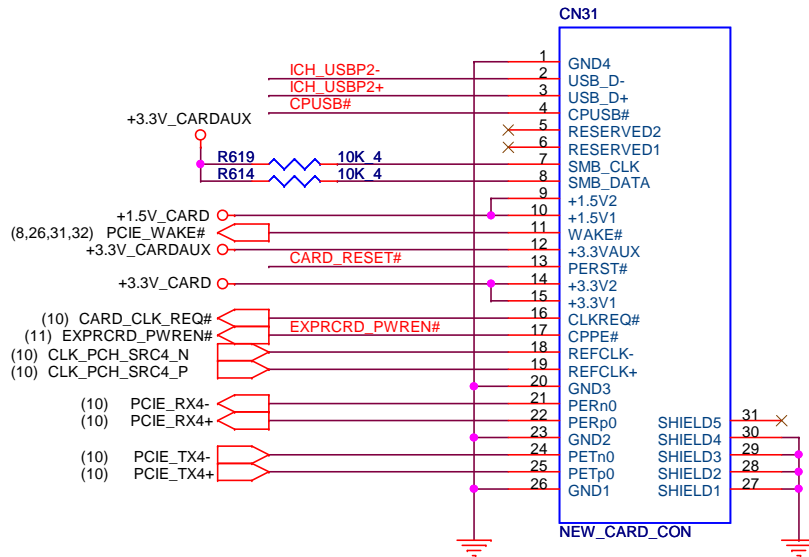
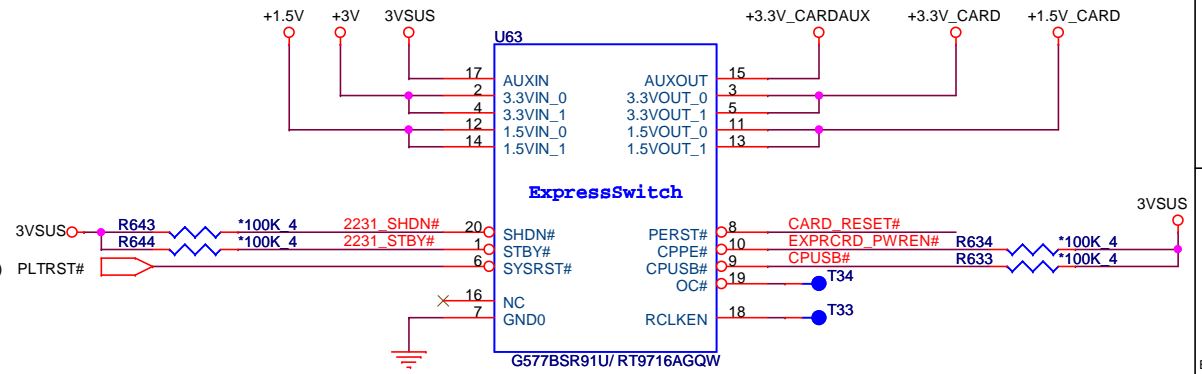
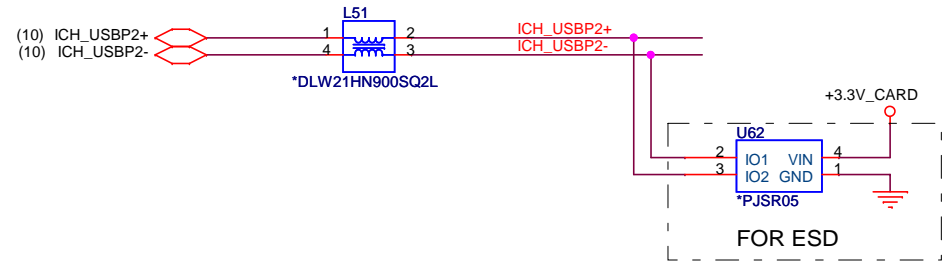


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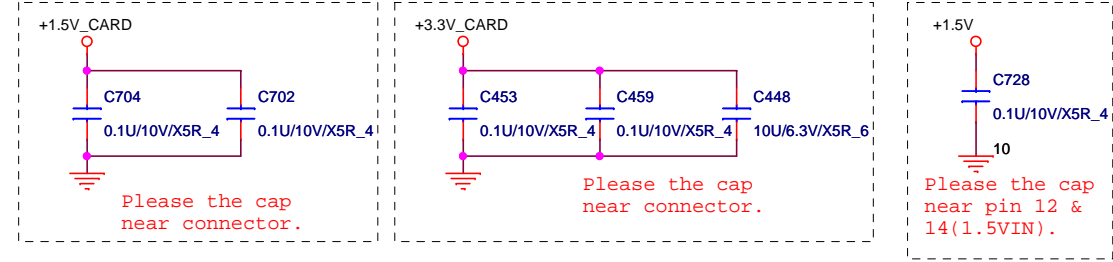
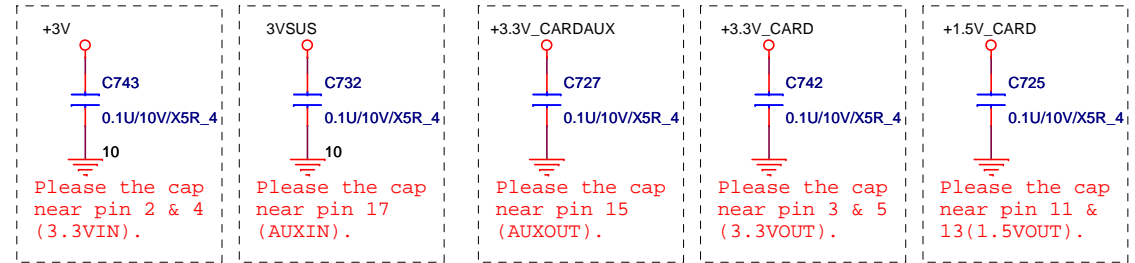
Express Card

(3,4,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,34,35,36,37,39,40,44,47) +3V
(31,32,41) +1.5V
(36,37,39,47,48) 3VSUS

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.
JAE PX10FS16PH-26P

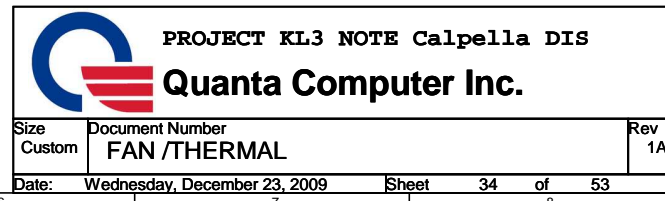
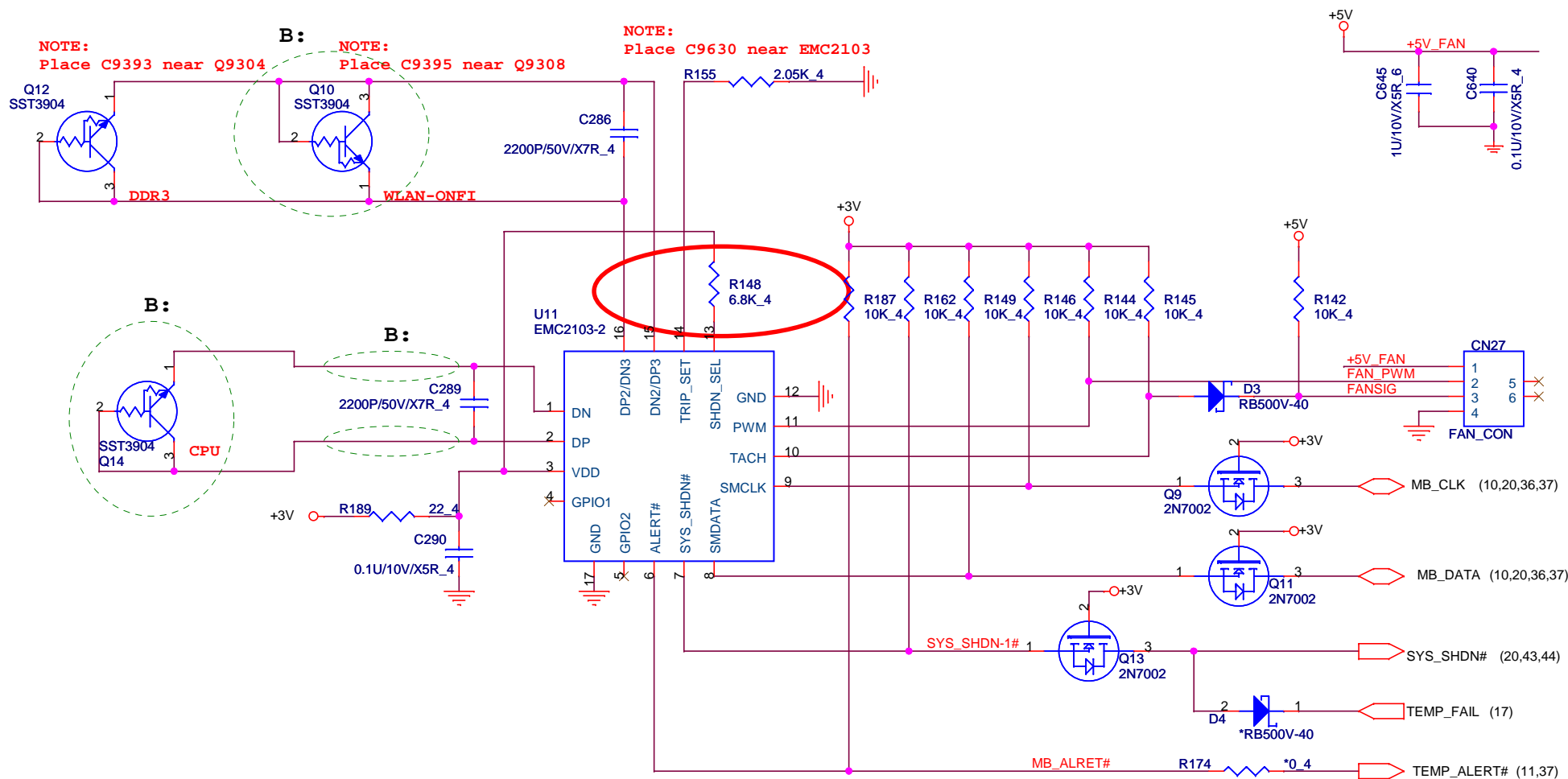


(3,4,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,35,36,37,39,40,44,47)
(12,23,24,25,27,28,35,37,39,40,44,47)

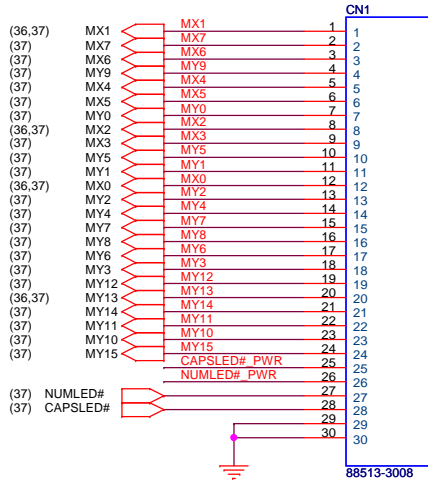
+3V
+5V



34

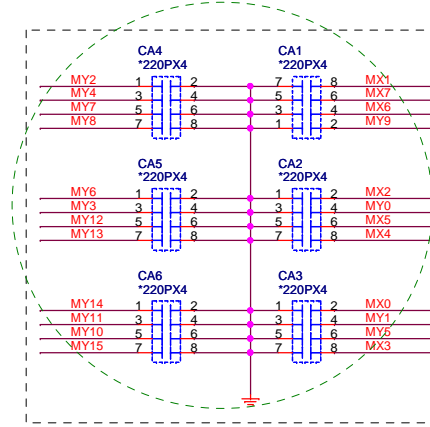


KEYBOARD



(12,23,24,25,27,28,34,37,39,40,45) +5V
(9,24,26,36,37,39,40,43,47) 3VPCU

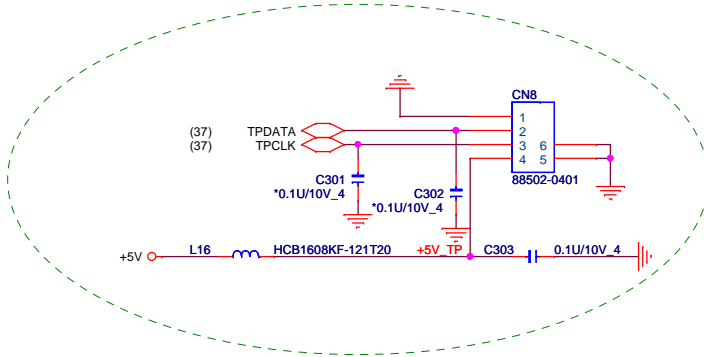
B:



For EMI request

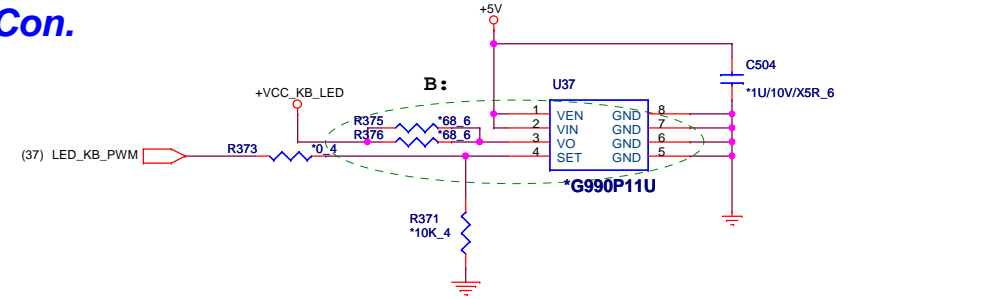
Touch pad

B:

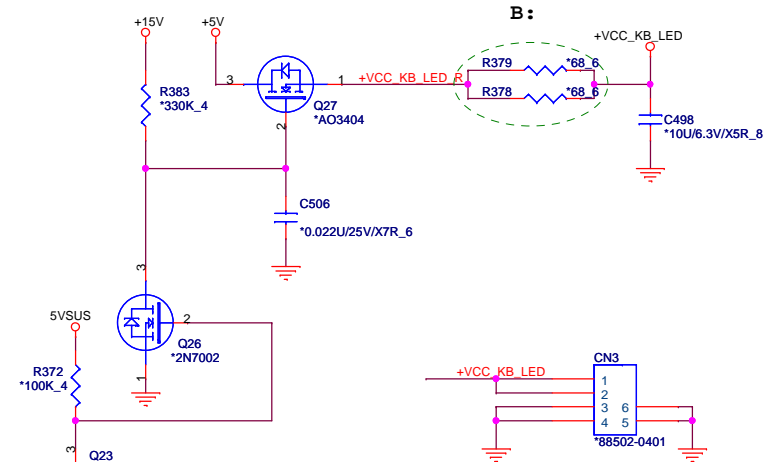


Backlight Keyboard Con.

B:

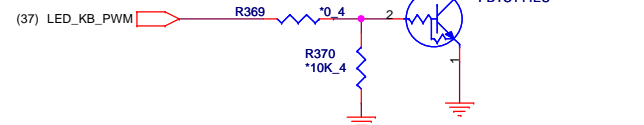


B:



EC PWM Pin

(37) LED_KB_PWM



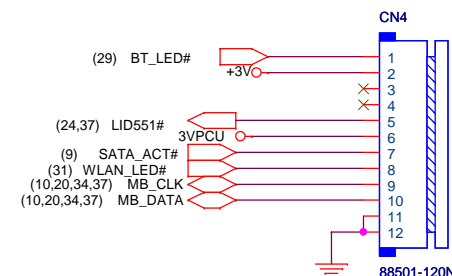
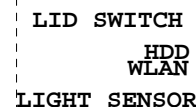
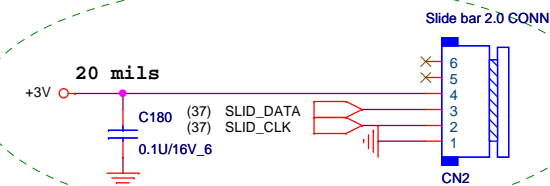
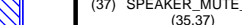


Diagram of the CN5 connector pin configuration:

- Pin 1: 3VPCU
- Pin 2: (X)
- Pin 3: (X)
- Pin 4: (37) PWR_WHITE#
- Pin 5: (37) NBSWON#
- Pin 6: (37) NOVOCARE_BUTTON#
- Pin 7: Ground
- Pin 8: Ground

Connector label: CN5
Part number: 88511-0841

(37) SPEAKER_MUTE_LED#

(35,37) MY13

(35,37) MX0

(35,37) MX1

(35,37) MX2

C674

C673

C651

C650

C287

220P/50V/XTR_4

220P/50V/XTR_4

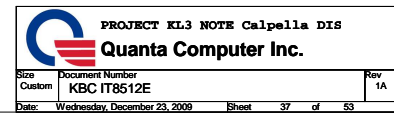
220P/50V/XTR_4

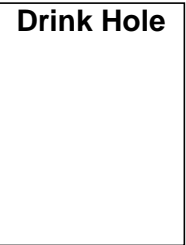
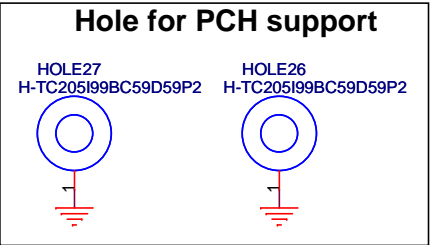
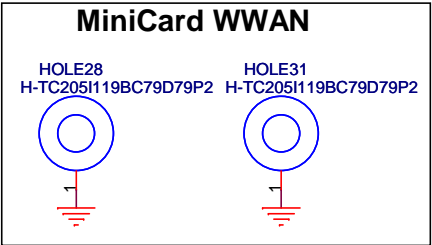
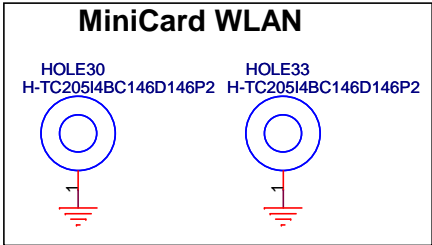
220P/50V/XTR_4

220P/50V/XTR_4

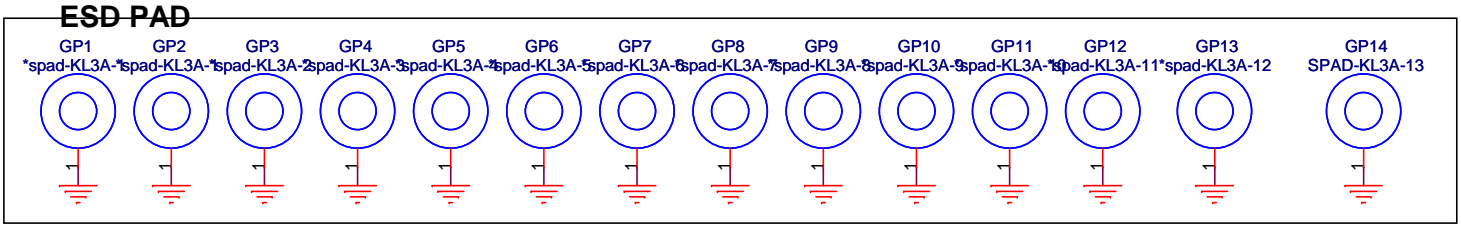
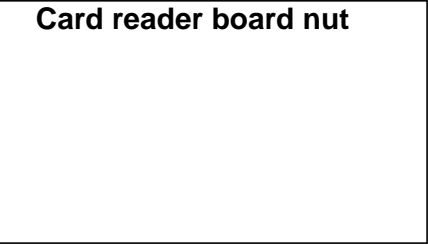
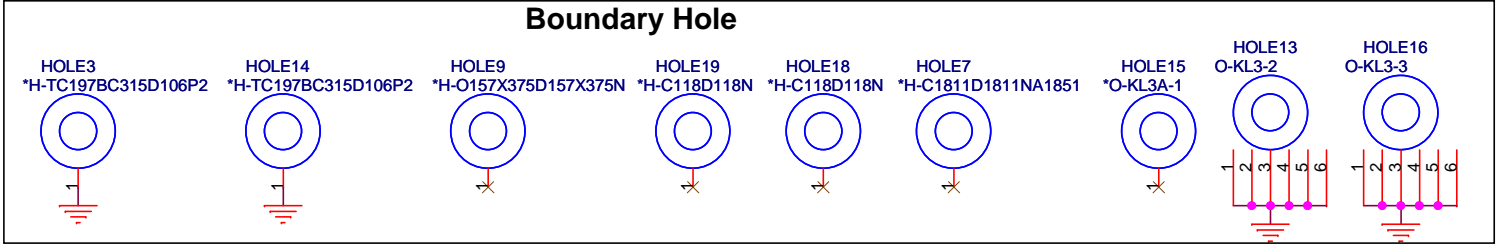
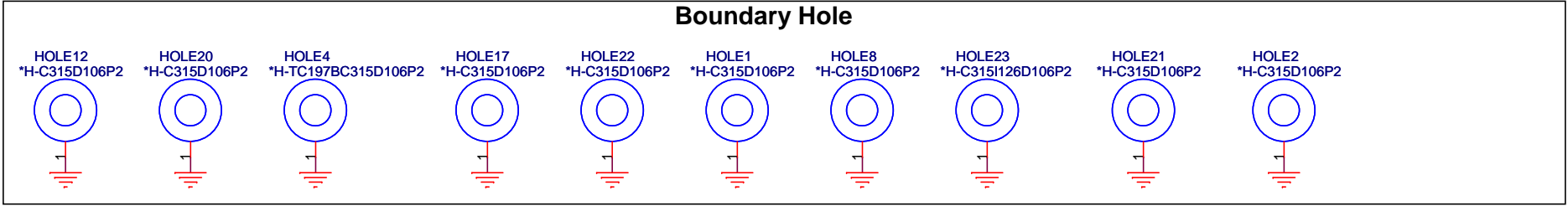
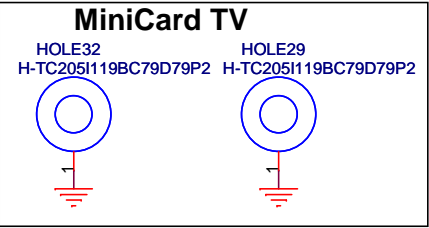
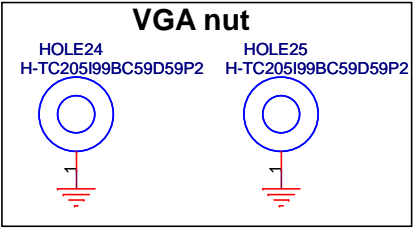
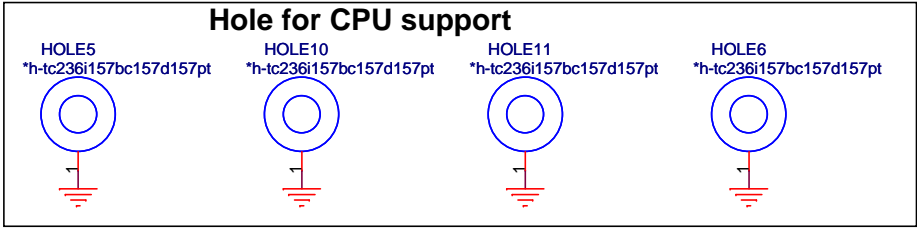
FOR EMI

88511-084





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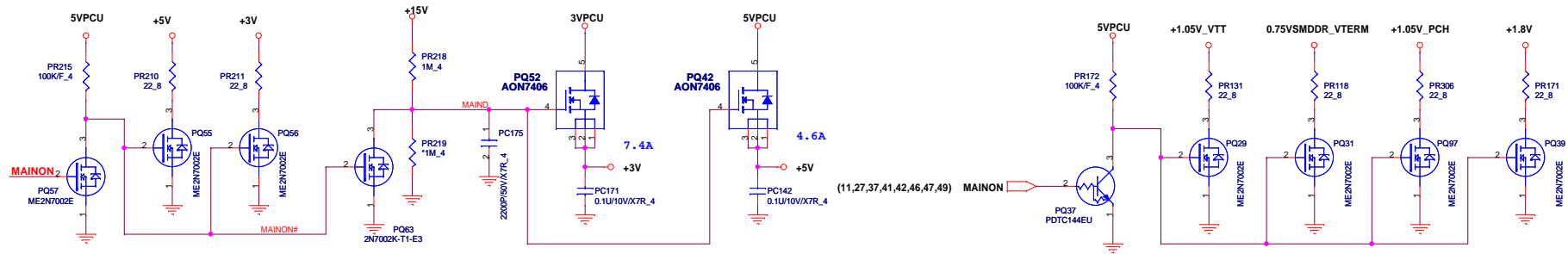


PROJECT KL3 NOTE Calpella DIS

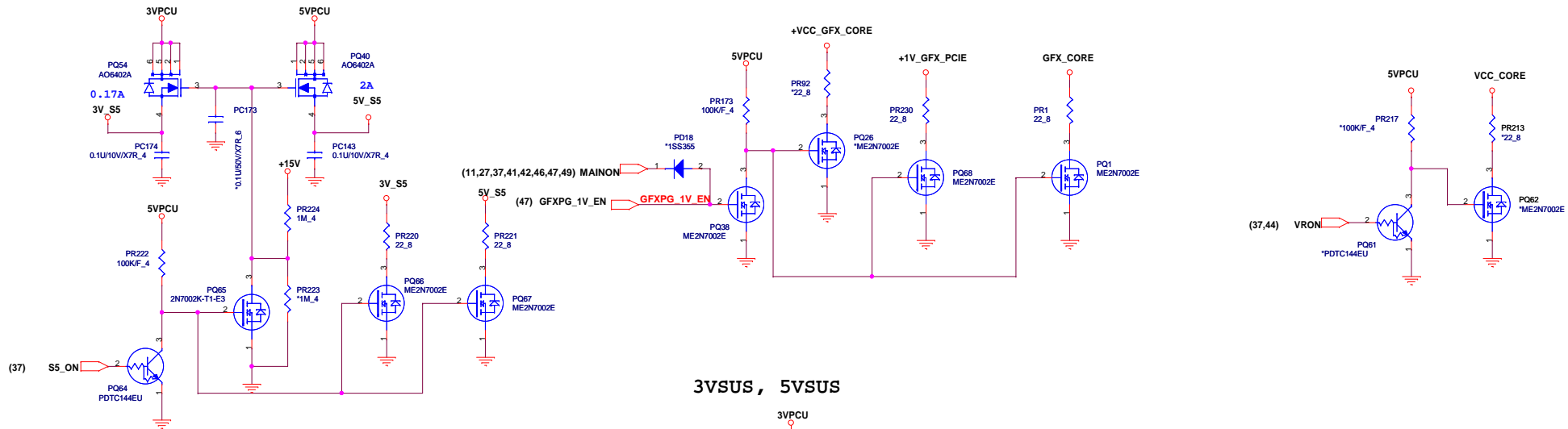
Quanta Computer Inc.

Size Custom	Document Number HOLD & SKEW	Rev 1A
Date: Wednesday, December 23, 2009	Sheet 38	of 53

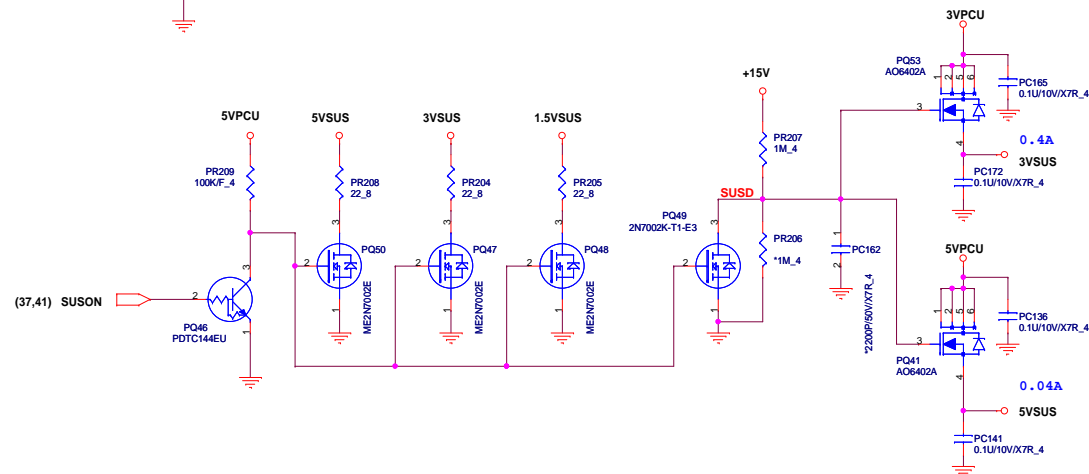
+3V, +5V



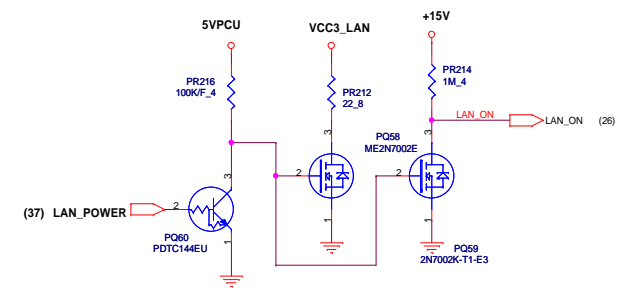
3V_S5, 5V_S5



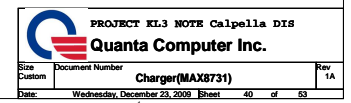
3VSUS, 5VSUS

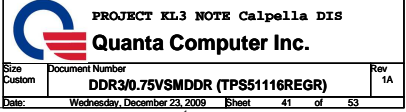


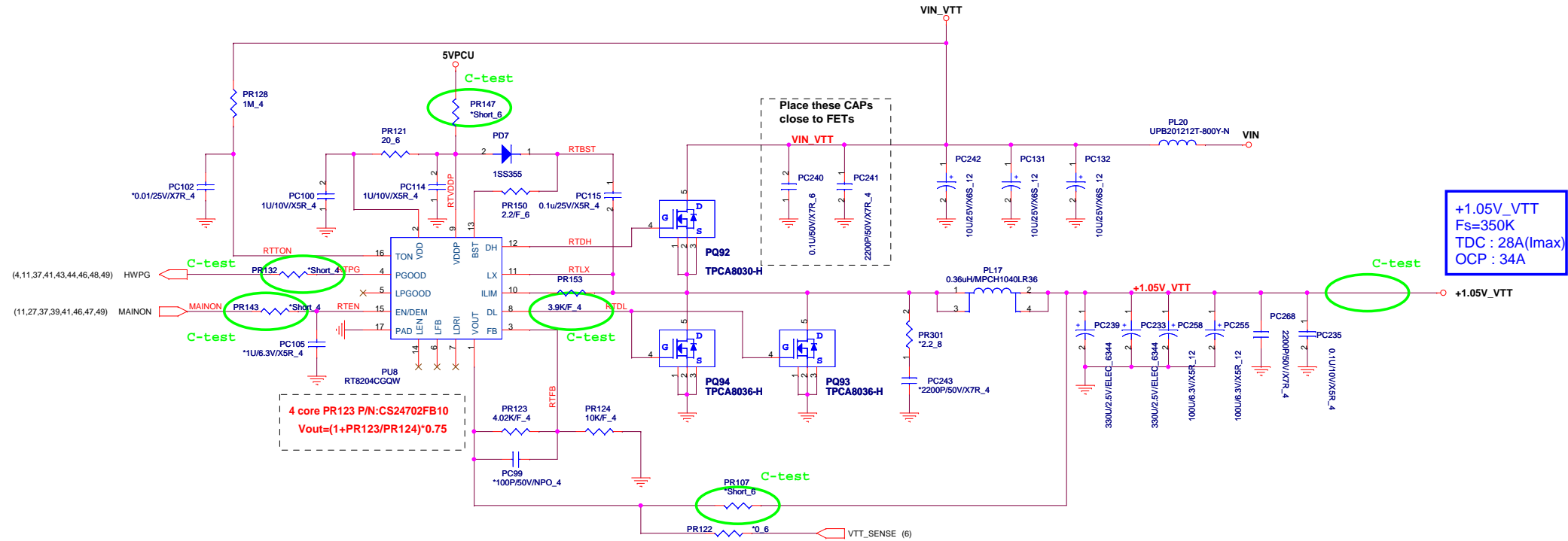
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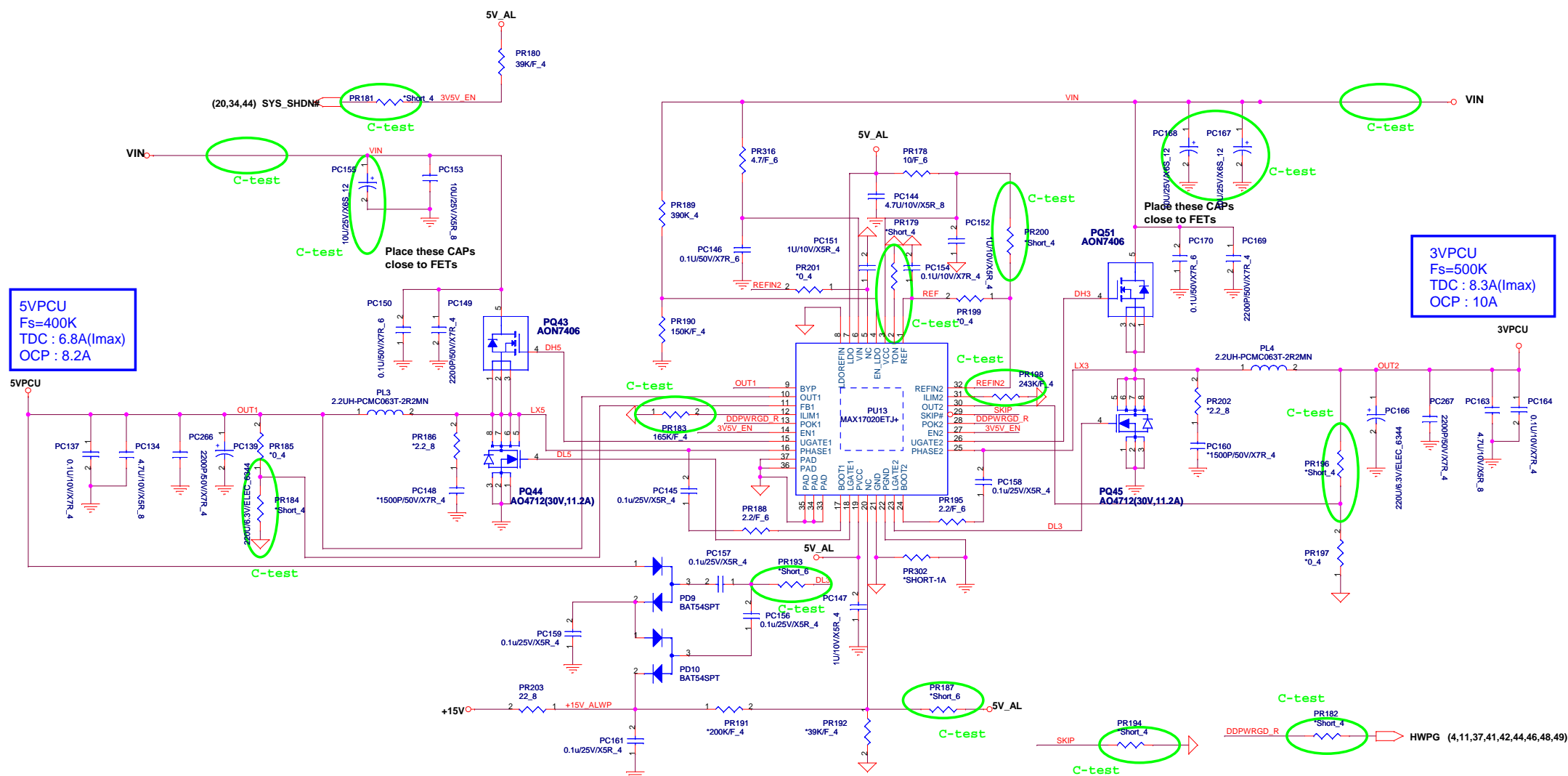


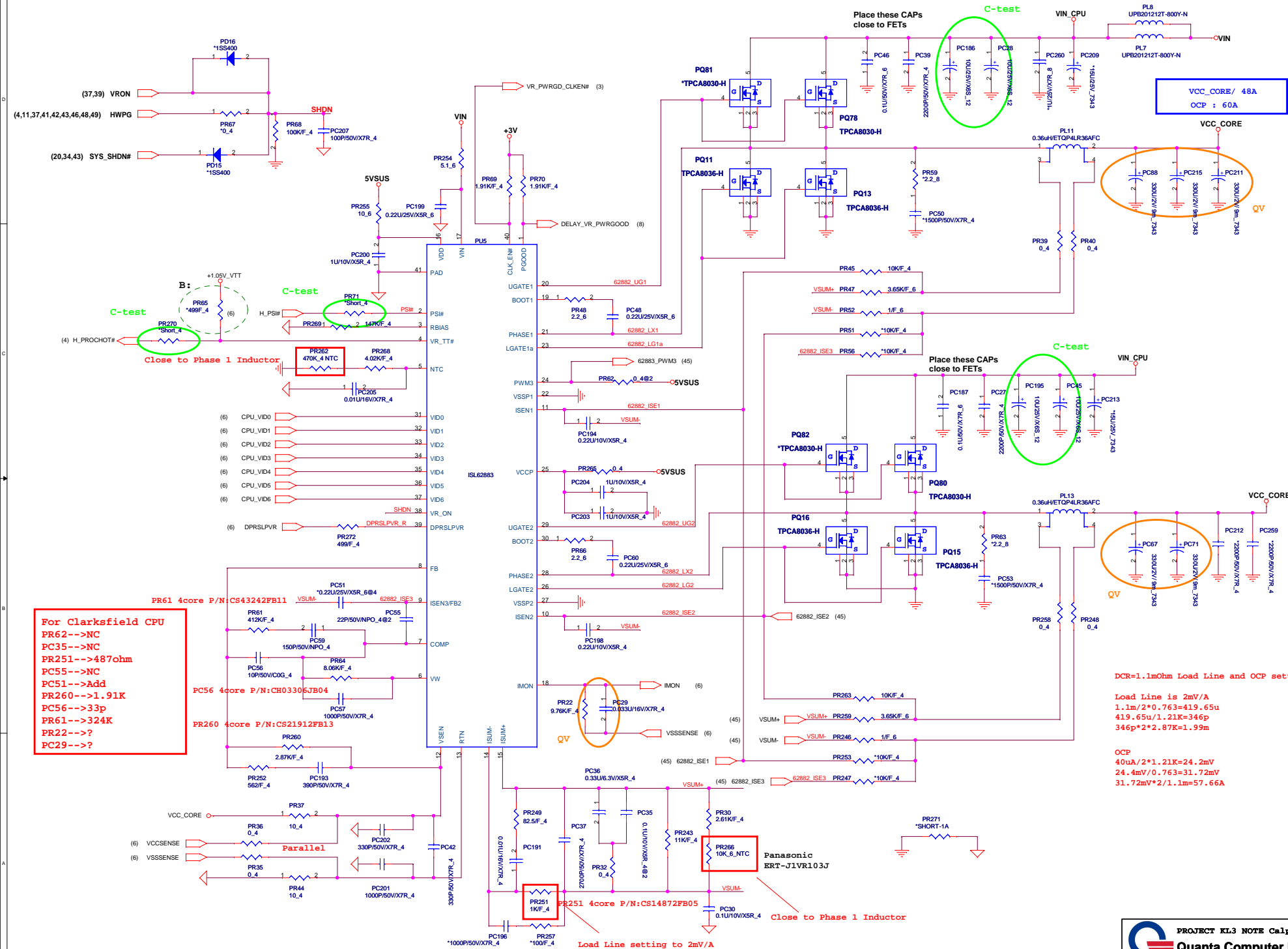
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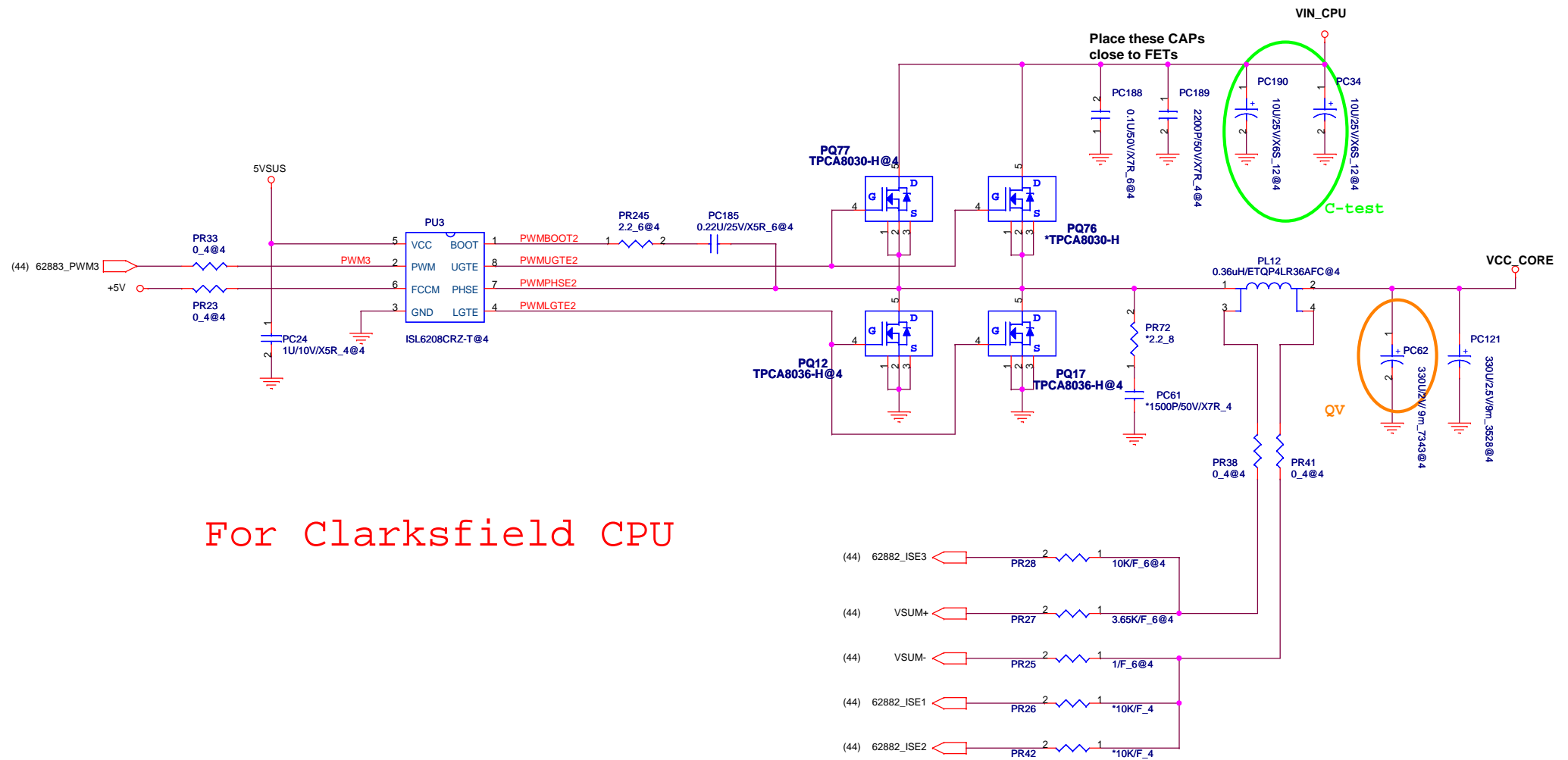


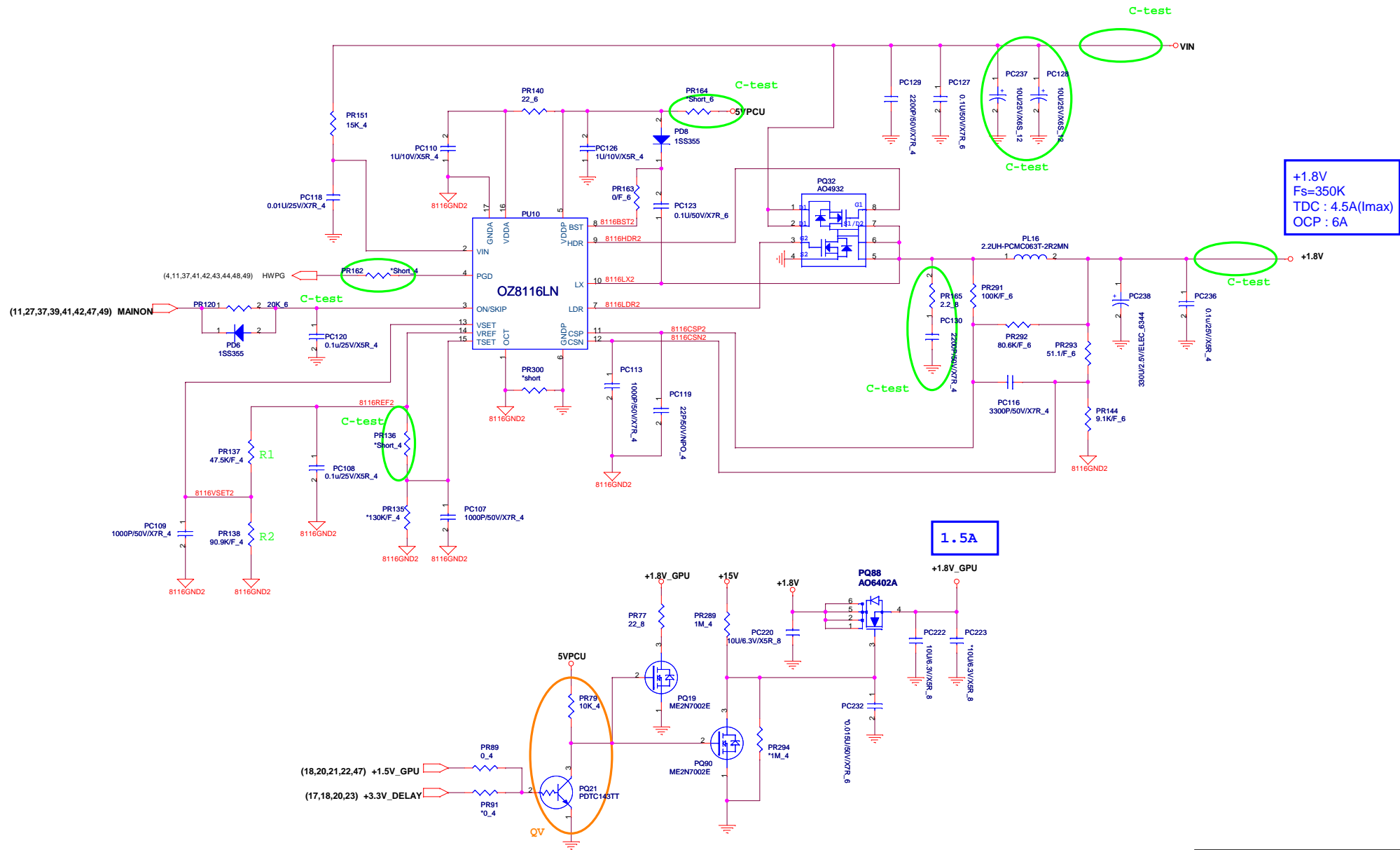


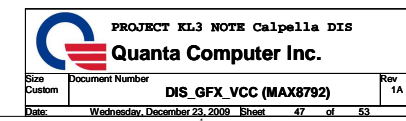


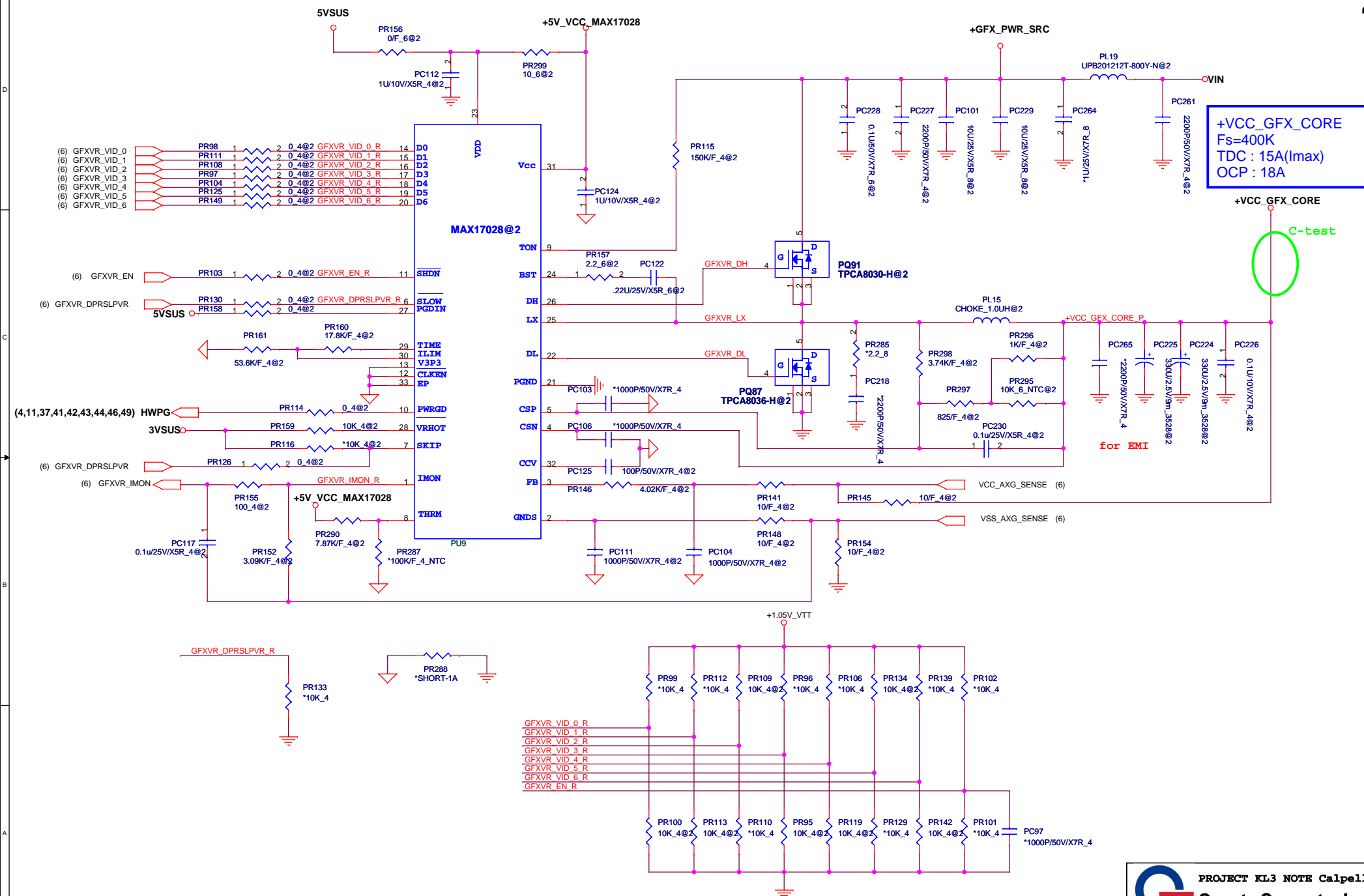












Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

[illegible]

EC #	Page	Description	Part Affected
EC-A-01	12	0 ohm change to DEL for reduce 1.05V drop	R261
EC-A-02	35	Change footprint and schematic for design request	CN5
EC-A-03	35	DEL R126 and connect CN5.25 to GND directly	R126
EC-A-04	38	Add 10 ohm for reduce noise	R577
EC-A-05	39	DEL CN2 for combine with GC4/GC5	CN2
EC-A-06	10	25MHz X'tal ICG support removed from POR	Y6,R478,C671,C670
EC-A-07	12	Based on Intel DG V1.5 page320, remove external LC filter for VCCAClk, VccapIEXP, VCCFDIPLL, VCCSATAPLL.	L45,C692,L46,C697,L47,C712, C715,L21,C329,C331
EC-A-08	14	Based on Intel DG V1.5 page100 ,remove DDR3 Vref control circuit M2 option.	U1 etc...
EC-A-09	15	Based on Intel DG V1.5 page100 ,remove DDR3 Vref control circuit M2 option.	U46 etc...
EC-A-10	23	Change from 0 ohm to bead for EMI request	R150
EC-A-11	26	Change from 0 ohm to bead for EMI request	R237,R238,R239,R240
EC-A-12	43	Del +1.05V_PCH discharge	PR219,PQ11
EC-A-13	43	Add charger PTC	PR263
EC-A-14	43	Change Footprint	PQ66
EC-A-15	43	Modify OTP circuit	PD34
EC-A-16	44	Del NO ASM circuit	PU16 etc...
EC-A-17	46	Del +1.05V_PCH circuit	PQ133 etc...
EC-A-18	46	Reduce +1.05V power rail impedance	PJP13,PJP4
EC-A-19	46	Reserve for current derating	PL23
EC-A-20	46	Reduce transient regulation	PL20
EC-A-21	47	Reduce ripple voltage	PC216
EC-A-22	49	Add to separate enable from protect circuit	PR264
EC-A-23	49	Reserve for sequence	PR265
EC-A-24	29	ESD suggestion because ESATA don't CDE test so we DEL U7,U8 and add a GND shielding in board file	U7,U8

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